APPENDIX A

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(Insert in 625-205, Galileo Orbiter Functional Requirements Book)

APPENDIX D

No. GLL-3-280
Appendix D to Revision D
15 August 1995

PHASE 2

FUNCTIONAL REQUIREMENT

GALILEO ORBITER

TELEMETRY MEASUREMENTS AND DATA FORMATS

Revised and Rewritten

Custodian:

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R. Johansen

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12/21/94 **CHANGE NOTES**

This first fully integrated issue of the GLL Phase 2 3-280 Telemetry Specification encompasses the sequential implementation of ECRs 35557, 35565, 35566, 35567, 35581, 35582, 35587 and 35593 to the 09/03/93 issue of the GLL Phase 1 3-280 Telemetry Specification.

Because these ECRs resulted in changes to 80+ percent of the pages in the baseline 3-280 document, no change line indications have been utilized in this initial phase 2 3-280 release.

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08/15/95

This issue retires all versions for Appendix C and supersedes previous distribution for Appendix D.

The major area of change in this update lies in Section 3.10 which provides the details of GLL Phase 2 Packetized Telemetry. Within 3.10 the sub-areas of interest are:

p. D-90 thru D-98 - Overview and Downlink Descriptions
p. D-99 thru D-137o - Detailed Packet Definitions
p. D-137p thru D-137u - Operating Modes & Controls

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APPENDIX A

TELEMETRY FRAME FORMAT

COMPONENTS

A1.0 SCOPE

This document establishes the Galileo (GLL) Orbiter requirement for telemetry measurements.

A2.0 TELEMETRY FRAME FORMAT COMPONENTS

A2.1 General

The following paragraphs contain the structure and contents of the elements comprising the various data formats found in GLL-3-280, paragraph 3.9.

A2.2 Engineering Data

The engineering data shall contain a fixed area and a variable area allocation for measurement sampling. The fixed allocation shall be invarient under all the GLL mission phases.

The variable area allocation shall accommodate the various mission phase sampling requirements including anomaly investigations, special tests, spacecraft system test, and performance monitoring. The engineering data shall be allocated as shown in Figure A2.2.1 and described in greater detail in Table A2.2.1.

(100 LEVEL DECK - LESS HEADER)

HLM 1A DATA	LLM 1A DATA	LMM 2A DATA	HLM 1B DATA	LLM 1B DATA	LLM2B DATA	AACS DATA	S P A R E	P1	P2	P3	P4	P5	P6	P7	P8	P9
40	48	16	40	48	16	128	8									

Figure A2.2.1. Engineering Data

A2.2.1 Measurement Position Identification. In order to assign measurements to the engineering data allocation, it is necessary to describe the structure and placement of measurements on the structure. The description must support the ability to command commutation map changes and to identify measurement position within the structure.

Within the fixed area and variable area, the structure location shall be as described in the following paragraphs.

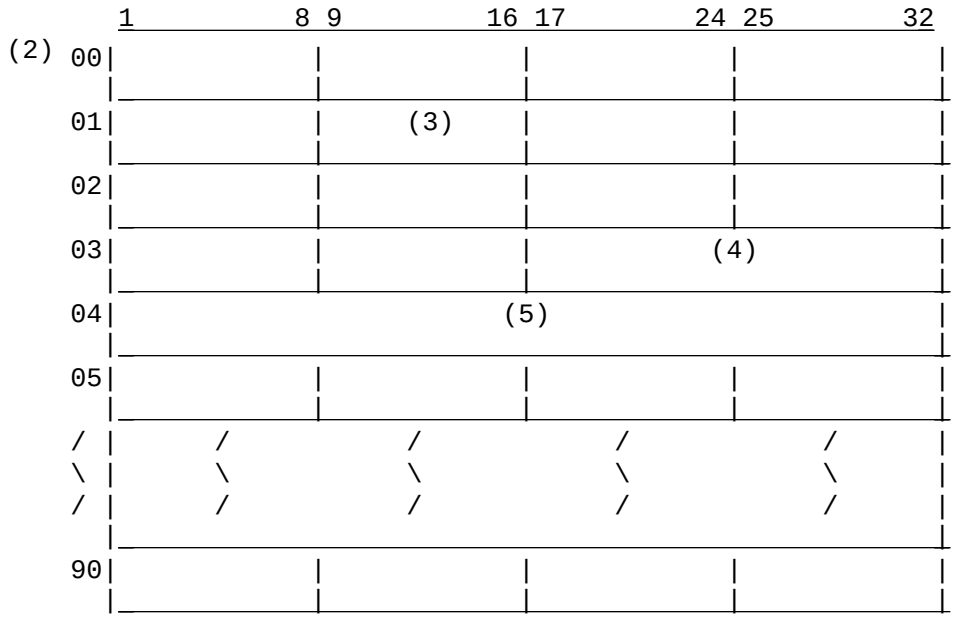
A2.2.1.1 Fixed-Area Allocation. Using the example in Figure A2.2.2 from HLM1A, the resulting structure and rules for creating the structure identifiers are highlighted.
The rules and legal values for creating the identifiers are shown in Table A2.2.2.

Table A2.2.1. Engineering Data

Data Description	Bits Frame	Offset to Data Start	Paragraph
High Level Module (HLM)1A Data	40	0	A2.2.2
Low Level Module (LLM)1A Data	48	40	A2.2.3
LLM 2A Data	16	88	A2.2.4
HLM 1B Data	40	104	A2.2.5
LLM 1B Data	48	144	A2.2.6
LLM 2B Data	16	192	A2.2.7
AACS Data	128	208	A2.2.8
spare	8	336	
Packet-1	40	344	A2.2.11
Packet-2	40	384	A2.2.11
Packet-3	40	424	A2.2.11
Packet-4	40	464	A2.2.11
Packet-5	40	504	A2.2.11
Packet-6	40	544	A2.2.11
Packet-7	40	584	A2.2.11
Packet-8	40	624	A2.2.11
Packet-9	40	664	A2.2.11
	704		

(1)
HLM-1A N1F

HLM-1A N1F



NOTES:

(1) THIS SUBCOM (N1F) IS OF LENGTH 91 ("N"), IS THE FIRST SUBCOM OF THIS TYPE IN HLM1A ("1"), AND IS FOUR BYTES WIDE.

(2) THIS IDENTIFIES THE SUBCOM POSITION.

(3) A MEASUREMENT IN THIS POSITION IS IDENTIFIED AS HLM1A N1F01 2.

(4) A MEASUREMENT IN THIS POSITION IS IDENTIFIED AS HLM1A N1F03 3. THE MEASUREMENT CONSISTS OF 16 BITS.

(5) A MEASUREMENT IN THIS POSITION IS IDENTIFIED AS HLM1A N1F04 1. THE MEASUREMENT CONSISTS OF 32 BITS.

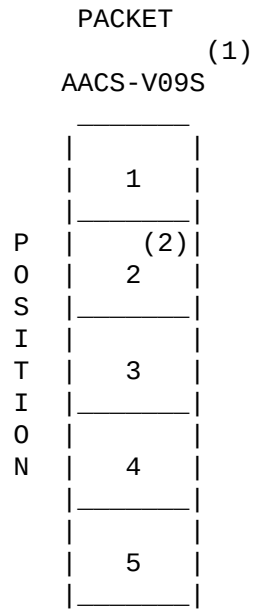
Figure A2.2.2. Fixed Area Structure/Position Identifiers

Table A2.2.2. Fixed Area Structure/Position Identifiers

Item	Item Identifier	Contents	Meaning	Comments
1.	Module ID	AACS HLM1A HLM1B LLM1A LLM1B LLM2A LLM2B		Identifies the module which creates the fixed area packet.
2.	Commutation Deck Length	Z S T N	One Seven Thirteen Ninety One	Indicates the repetition cycle of the data; e.g., every "n"th frame.
3.	Number of Commutation Deck of this Type	$1 \leq m \leq M$		Sequential number of commutator deck length and width (items 2 and 4).
4.	Commutation Deck Width	S D F	Single Byte Double Byte Four Byte	Width of Structure
5.	Position in Commutator Deck	See Comments		Item 2 — Maximum Value: Z — 0 S — 6 T — 12 N — 90
6.	Measurement Characteristic	1 2 3 4	First Byte Second Byte Third Byte Fourth Byte	In multiple byte subcoms, this indicates the position of the measurement in the subcom. Measurements consisting of more than one byte are identified by the position of the most significant byte.

A2.2.1.2 Variable-Area Allocation. Using the example in Figure A2.2.3 for a typical AACS variable area packet, the resulting structure and the rules for creating the structure/position identifiers are highlighted.

The rules and allowed values for creating the identifiers are shown in Table A2.2.3.



NOTES:
(1) THE ILLUSTRATED 5 BYTE PACKET IS THE NINTH ("09") VARIABLE ("V") PACKET FROM "AACS". EACH MEASUREMENT IS NOMINALLY ONE BYTE ("S").
(2) A MEASUREMENT IS PLACED IN POSITION "2" OF THE VARIABLE PACKET
- (a) TO IDENTIFY A SINGLE BYTE ASSIGNMENT IN THIS LOCATION, THE POSITION IDENTIFIER IS AACS-V09S2F
- (b) TO IDENTIFY A TWO BYTE ASSIGNMENT IN THIS LOCATION, THE POSITION IDENTIFIER IS AACS-V09S2D
- (c) TO IDENTIFY ONE HALF OF A TWO BYTE ASSIGNMENT IN THIS LOCATION,THE POSITION IDENTIFIER IS
  AACS-V09S2L (LEFT BYTE) OR
  AACS-V09S2R(RIGHT BYTE)

Figure A2.2.3. Variable Area Packet Structure/Position Identifiers

Table A2.2.3. Variable Area Packet Structure/Position Identifiers

Item	Identifier	Contents	Meaning	Comments
1	Module ID	AACS		Identifies the module which creates the variable area packet
		HLM 1A		
		HLM 1B		
		LLM 1A		
		LLM 1B		
		LLM 2A		
		LLM 2B		
2	Variable Packet	V	Variable area packet of length 5	Used to differentiate between fixed area and variable area packets
3	Packet number	01 ≤ n ≤ 16		Identifies the specific packet within the module of interest
4	Width	S	Single Byte	
	Description stops here if desire is to just identify packet. To identify a specific position, the remaining items are used.			
5	Packet Position	1 ≤ positions ≤ 5		Position within packet
6	Measurement Characteristic	F	1 byte measurement	
		D	2 byte measurement	Packet position ≤ 4
		L	Left byte	Left byte of 2 byte measurement assigned to specific packet position
		R	Right byte	Right byte of 2 byte measurement assigned to specific packet position

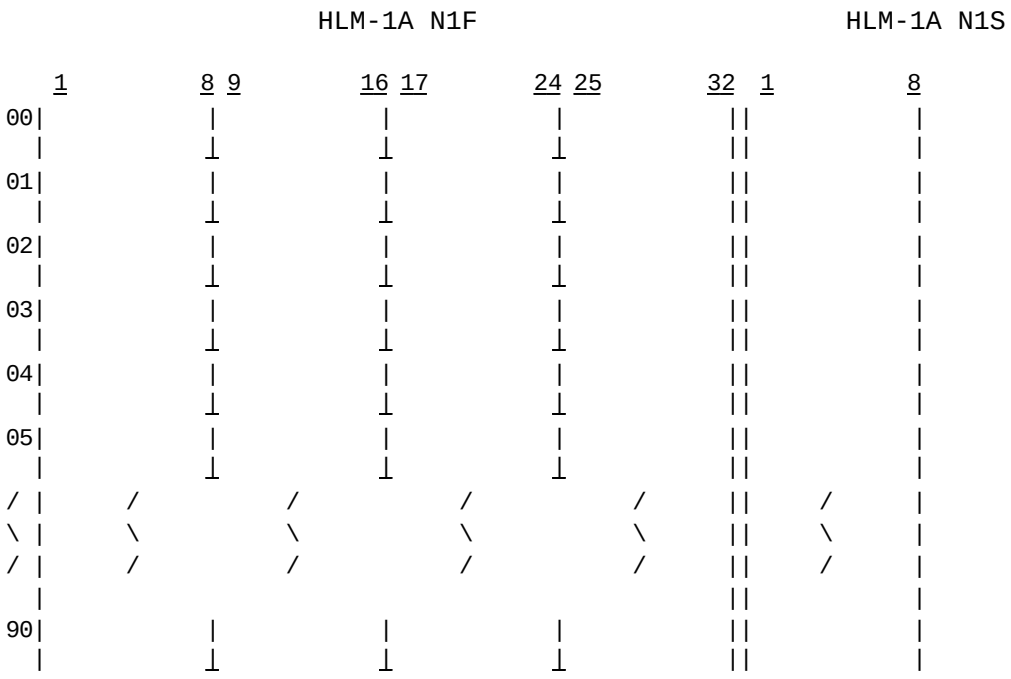


Figure A2.2.4. HLM 1A Data Packet

A2.2.2 High Level Module 1A Data Packet. The fixed area allocation for HLM 1A shall contain those measurements created within or sampled by HLM 1A.

The structure associated with the HLM 1A data shall be as shown in Figure A2.2.4 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown in the figure).

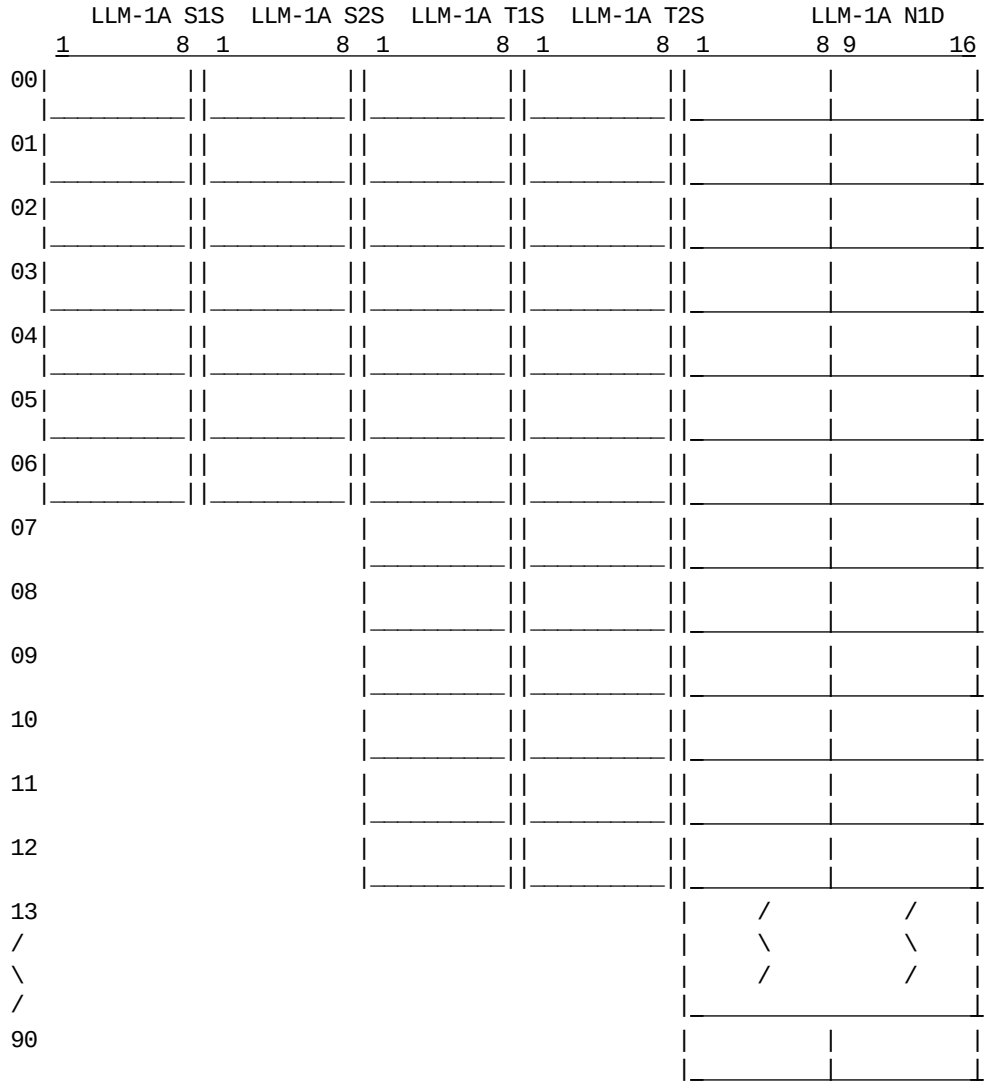


Figure A2.2.5. LLM 1A Data Packet

A2.2.3 Low Level Module 1A Data Packet. The fixed area allocation for LLM 1A shall contain those measurements created within or sampled by LLM 1A.

The structure associated with LLM 1A data shall be as shown by Figure A2.2.5 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown on the figure).

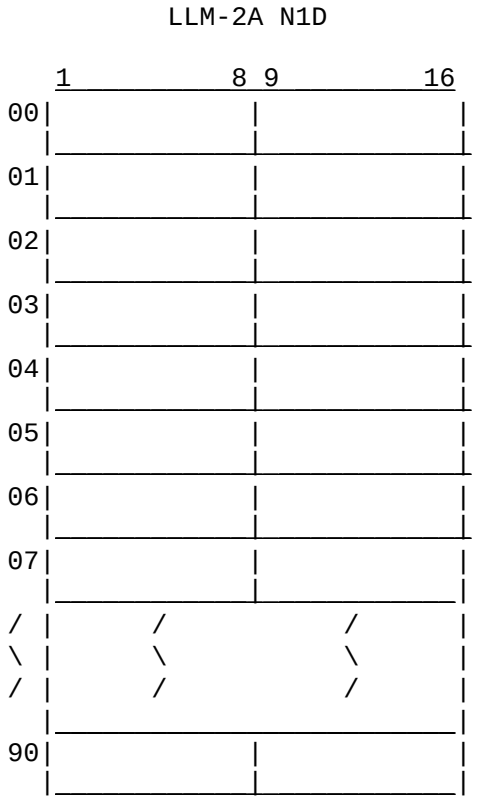


Figure A2.2.6. LLM 2A Data Packet

A2.2.4 Low Level Module 2A Data Packet. The fixed area allocation for LLM 2A shall contain those digital or software measurements created within or sampled by LLM 2A. Analog measurements on the despun side of the spacecraft shall be sampled by either LLM 2A or LLM 2B depending on the spacecraft hardware configuration.

The structure associated with LLM 2A data shall be as shown by the Figure A2.2.6 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown on the figure).

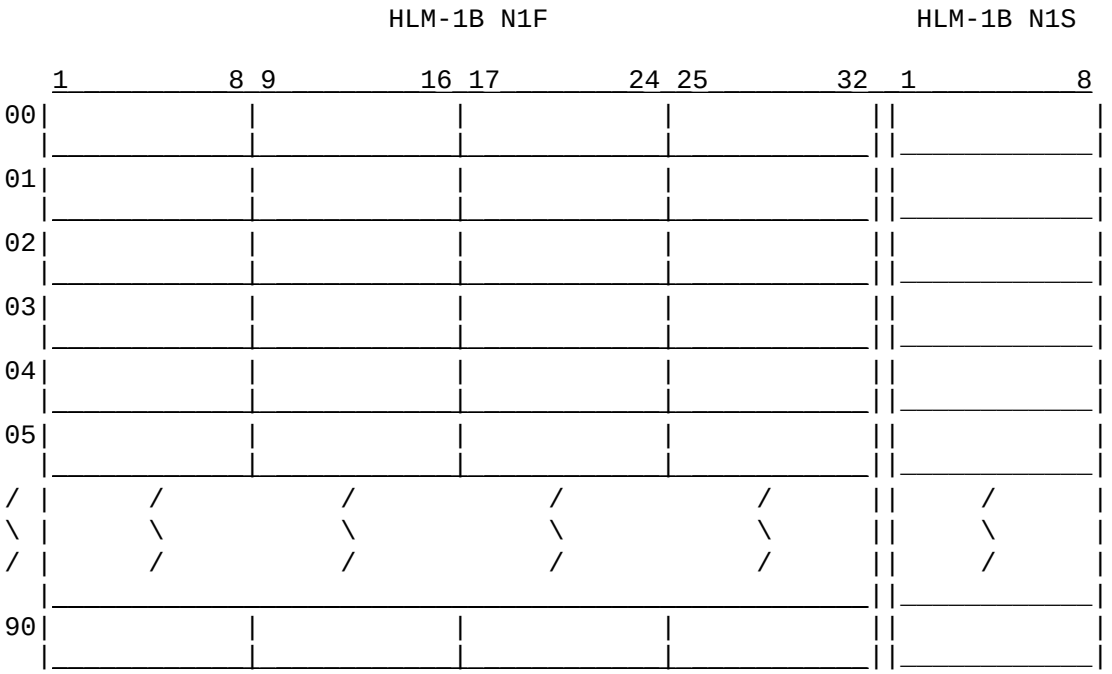


Figure A2.2.7. HLM 1B Data Packet

A2.2.5 High Level Module 1B Data Packet. The fixed area allocation for HLM 1B shall contain those measurements created within or sampled by HLM 1B.

The structure associated with HLM 1B data shall be as shown by Figure A2.2.7 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown in the figure).

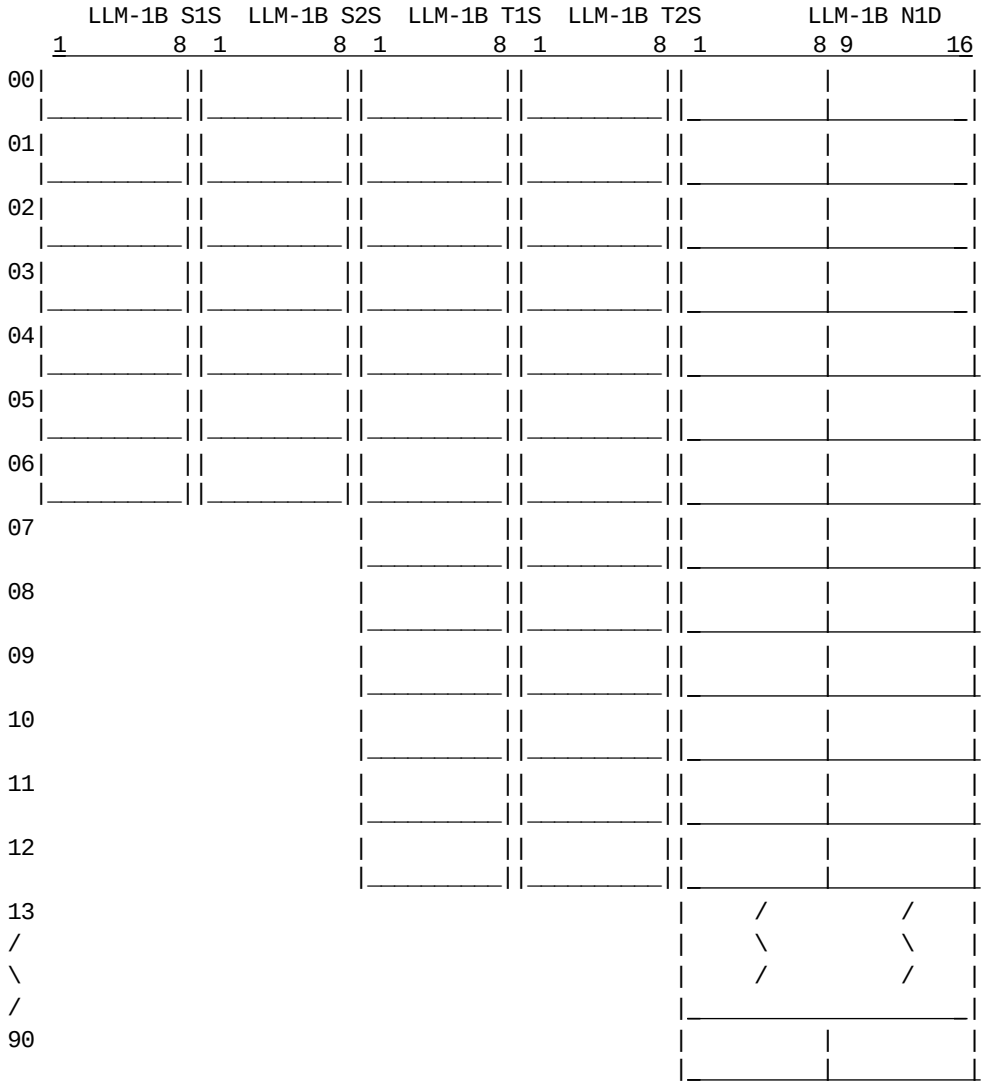


Figure A2.2.8. LLM 1B Data Packet

A2.2.6 Low Level Module 1B Data Packet. The fixed area allocation for LLM 1B shall contain those measurements created within or sampled by LLM 1B.

The structure associated with LLM 1B data shall be as shown by the Figure A2.2.8 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown on the figure).

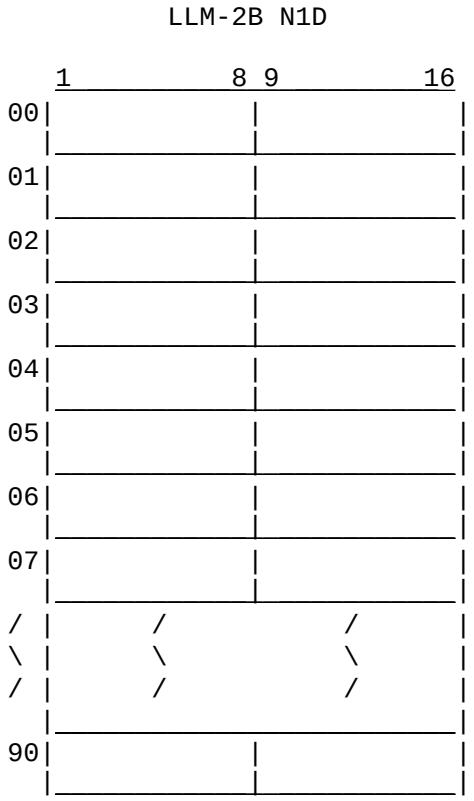


Figure A2.2.9. LLM 2B Data Packet

A2.2.7 Low Level Module 2B Data Packet. The fixed allocation for LLM 2B shall contain those digital or software measurements created within or sampled by LLM 2B. Analog measurements on the despun side of the spacecraft shall be sampled by either LLM 2A or LLM 2B depending on the spacecraft hardware configuration.

The structure associated with LLM 2B data shall be as shown by the Figure A2.2.9 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown in the figure).

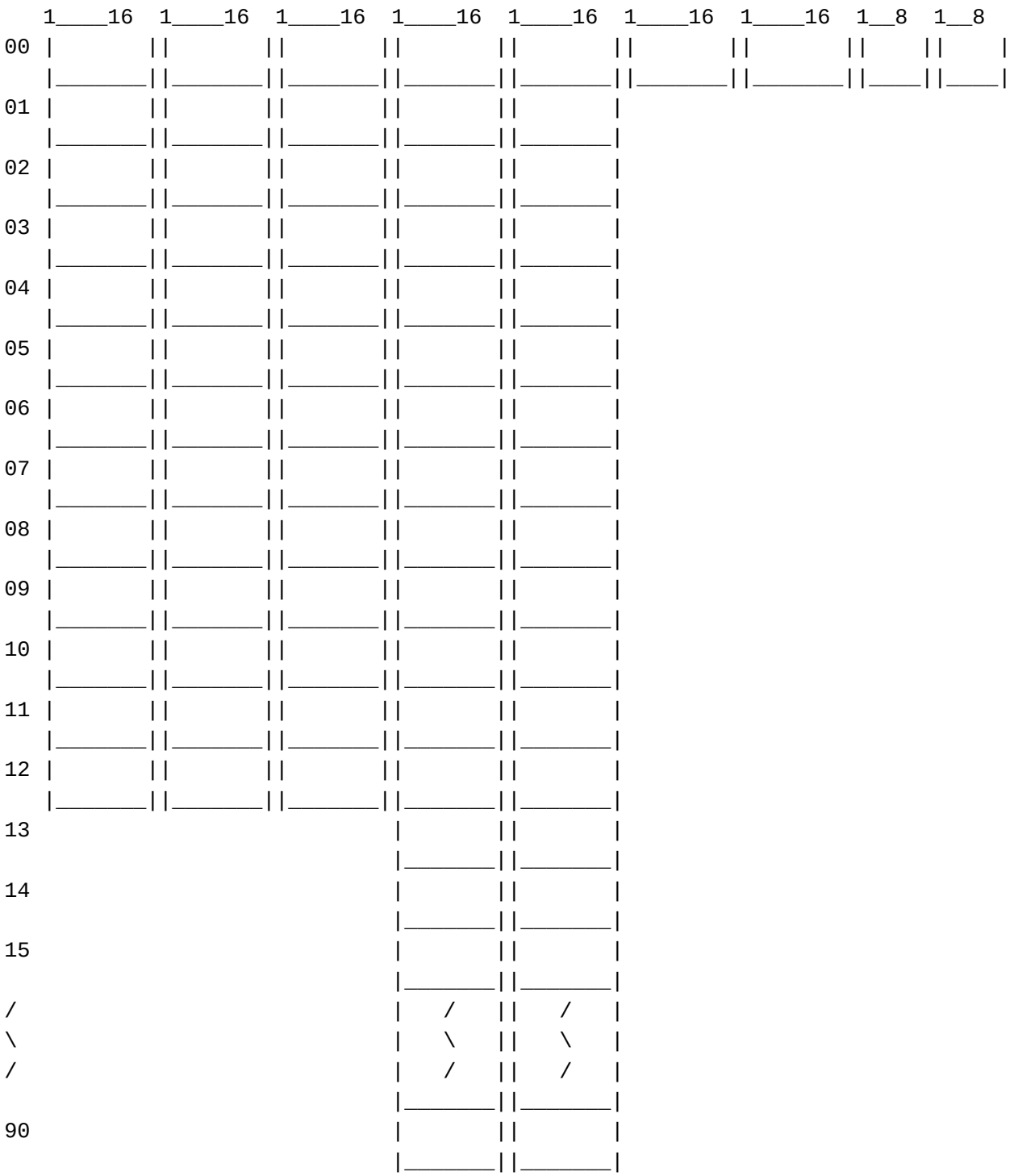


Figure A2.2.10. AACS Data Packet

A2.2.8 Attitude and Articulation Control Subsystem Data Packet. The fixed area allocation for the AACS shall contain those measurements created within or sampled by AACS.

The structure associated with AACS data shall be as shown by Figure A2.2.10 (refer to paragraph A2.2.1.1 for the interpretation of the identifiers shown in the figure).

A2.2.9 DELETED

A2.2.10 DELETED

MODULE-VnnS

	1	2	3	4	5
POSITION NUMBER					
BITS	8	8	8	8	8

1 40

Figure A2.2.11. Variable Packet

A2.2.11 Variable Area Packets. The variable area packets shall be identical in structure within each of the CDS and AACS computer modules. These packets shall accommodate the various mission phase differences in measurement sampling requirements.

The structure associated with each packet shall be as shown in Figure A2.2.11 (refer to paragraph A2.2.1.2 for the interpretation of the identifiers shown in the figure).

In any variable packet it shall be prohibited to create subcommutators within any position of the packet. There shall be no restriction as to the measurements which may be assigned to these packets.

A2.2.12 Measurement Sampling Times. The measurements placed into the engineering packet shall be sampled as specified in the succeeding paragraphs.

A2.2.12.1 Fixed Area Measurement Timing: CDS. Data sampled by a CDS High Level Module shall be sampled as specified in A2.2.12.1.1. Data sampled by a CDS Low Level Module shall be sampled as specified in A2.2.12.1.2.

A2.2.12.1.1 CDS High Level Module Sampling. Within the CDS, the data subcommutated into the HLM area of an engineering frame shall have been sampled during the MOD91=89 of the RIM previous to the RIM contained in the header.

A2.2.12.1.2 CDS Low Level Module Sampling. Within the CDS, software measurements subcommutated into the LLM area of an engineering frame shall have been sampled during the MOD91=89 of the RIM previous to the RIM contained in the header. The exceptions are the DMS Position Estimates (E-0423. E-0424, E-0923, and E-0924), and the Discharge Controller Use Counter (E-0089). These are sampled in the MOD91 previous to the MOD91 contained in the header. Hardware measurements (Analog, Digital, and Temperature) shall be sampled as shown in Table A2.2.4.

Table A2.2.4. CDS Fixed Area Measurement Sampling Time
(Milliseconds offset prior to SCLK)

Telemetry Mode	Rate b/s	Subcommutation Deck: S1S	S2S	T1S	T2S	N1D Left Byte	N1D Right Byte
1200 b/s	1200	646-2/3	580	446-2/3	380	246-2/3	180

Table A2.2.5. CDS Variable Packet Measurement Sampling Time
(milliseconds offset prior to SCLK)

Packet(1) Timing Position	Position Within Packet: 1	2	3	4	5
A	666-2/3	533-1/3	400	266-2/3	133-1/3
B	633-1/3	500	366-2/3	233-1/3	100
C	600	466-2/3	333-1/3	200	66-2/3
D	566-2/3	433-1/3	300	166-2/3	33-1/3
E	653-1/3	520	386-2/3	253-1/3	120
F	606-2/3	473-1/3	340	206-2/3	73-1/3
G	586-2/3	453-1/3	320	186-2/3	53-1/3
H	540	406-2/3	273-1/3	140	6-2/3
I	460	440	426-2/3	420	413-1/3

(1) In creating an engineering map, any of the packets ($01 \leq n \leq 16$) within a module may be assigned to the packet timing position A, B, C, D, E, F, G,

H, I.

A2.2.12.2 Variable Packet Measurement Timing: CDS. Within any CDS module creating variable area packets, the sample time relationship shown in Table A2.2.5 shall be maintained.

A2.2.12.3 Measurement Timing: AACS. Within the AACS, the data sampling shall occur during RTI 0 (MOD 10=0).

Table A2.2.6

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A2.2.13 S/C High Rate Sampling.

A2.2.13.1 CDS Single Identifier (SID) Mode. In order to assist in the investigation of spacecraft anomalies, it shall be possible to replace all of the variable engineering data with a single measurement. The measurement will be placed in all five positions of a packet, and then that packet shall occupy all timing positions shown in Table A2.2.5.

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A2.2.13.2 AACS Flood Mode. The AACS shall not be required to originate single- ID telemetry (hog-mode). Instead, for calibration of more volatile AACS measurements, a calibration measurement readout, popularly called "flood-mode" telemetry, shall be provided. The AACS shall at all times collect 6 measurements, in a 61 word rotating buffer, every 66 2/3 msec. The 6 measurements to be collected shall be capable of being specified by uplink commands. The MSS shall be provided with the ability to collect the AACS calibration buffer from the AACS and accumulate it in a larger buffer in the CDS once every 2/3 sec. for a period of up to 28 seconds, by means of an uplinked command sequence. Then the accumulated CDS buffer shall be transmitted to the ground by means of the standard memory readout telemetry capability, as the final step in the command sequence. The scheduling of a

calibration readout sequence shall be constrained by other sequencing events to those periods when the CDS accumulation buffer can be made available.

A2.2.14 Engineering Measurements and Formats

This section identifies the GLL engineering measurements, engineering formats, and commutator position assignments of each measurement within the engineering formats.

A2.2.14.1 Engineering Measurement Detailed Data

Table A2.2.8 provides detailed data for each engineering measurement. This data includes measurement engineering number (E-No.), title, identification (treeswitch or other identification, as appropriate), engineering unit range, number of bits, and type (analog/temperature/digital/software).

The table headings are as follows: NUMBER refers to engineering number. MEASUREMENT TITLE is the name of the measurement. ENGINEERING RANGE refers to the engineering range of the measurement, with degrees given in Celsius for temperature measurements. TREE POS refers to the hardware treeswitch position. COMM POS refers to the position in the engineering commutator, and therefore the frequency of sampling, of engineering measurements. NO. OF BITS indicates how many bits the measurement contains. FLAGS refers to 2 flags, with the first flag (F, V, or B) referring to whether the measurement is in the fixed commutator area only, the variable commutator area only, or both. The second flag (A, T, D, or S) denotes whether the measurement is an analog measurement, a temperature measurement, a digital measurement, or a software measurement.

Digital and Software bit definitions are shown in Table A2.2.9.

Eight despun measurements are multiplexed into the back-up despun measurement (BDM) channels (E-1109, E-1110, E-1129, E-1130). The multiplexing is controlled using 3 bits in the despun CRC registers known as the "Despun CRC backup mux select bits A, B, and C" as shown in Table A2.2.7.

Table A2.2.7. Backup Multiplexed Measurements

DESPUN CRC BACK-UP MUX SELECT BIT			CHANNEL ASSIGNMENT	MEASUREMENT SELECTED
C	B	A		
0	0	0	BDM 00	RRA position pot. 2
0	0	1	BDM 01	spare measurement
0	1	0	BDM 02	CDS +3VDC to RRA pot. 1
0	1	1	BDM 03	CDS despun commutator tree out
1	0	0	BDM 04	CDS despun signal ground
1	0	1	BDM 05	CDS filter calibration voltage
1	1	0	BDM 06	Unused
1	1	1	BDM 07	Unused

Measurements from the contamination monitor are multiplexed through channel E-0016. The CM's multiplexer is unsynched to the CDS and utilyzes two reference voltage states (0 and 3 volts) at the start of each data cycle to enable MOS to reconstruct the data. Each CM multiplexer state lasts for 3 minutes. The multiplexer states are described in Table A2.2.7A.

Table A2.2.7A CM Multiplexed Measurements

Multiplexer State	Measurement
0	0 volt reference (used to sync CM data)
1	3 volt reference (used to sync CM data)
2	QCM 1 output frequency
3	QCM 1 temperature measurement
4	QCM 2 output frequency
5	QCM 2 temperature measurement
6	QCM 3 output frequency
7	QCM 3 temperature measurement

A2.2.14.2 Engineering Formats

There are 5 GLL engineering formats, four of which are on the S/C at any one time. These formats are: anomaly, launch phase 1, launch phase 2, cruise/encounter/orbital operations, and maneuver/all spin. Each of these formats consists of a fixed area containing measurements common to all formats, and a variable area, containing packets of measurements unique to the specific format. Figure A2.2.12 provides an overview of the engineering commutator structure, showing the fixed and variable areas. The paragraphs that follow indicate the assignment of measurements to specific commutator positions within the fixed and variable areas.

A2.2.14.2.1 Fixed Area Measurement Assignments

Figures A2.2.13 through A2.2.19 indicate the commutator positions assigned to measurements in the fixed area.

*****SEE YOUR LIBRARY HARDCOPY FOR*****

Figure A2.2.12 Engineering Telemetry Commutator Structure (a foldout)

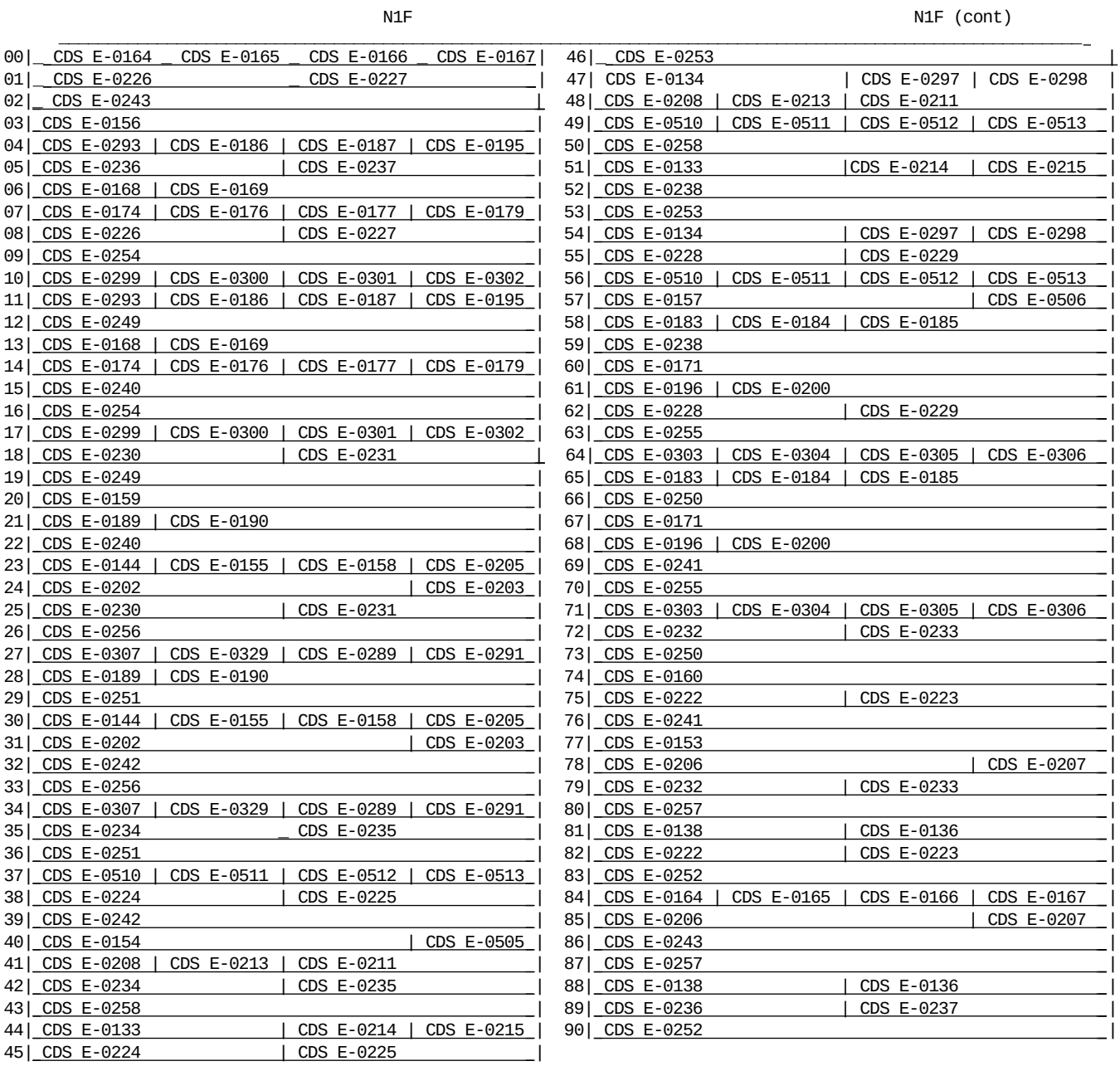


Figure A2.2.13. Fixed Area Measurement Assignment - HLM1A

N1S

00	CDS E-0162
01	CDS E-0322
02	CDS E-0509
03	CDS E-0321
04	CDS E-0508
05	CDS E-0163
06	CDS E-0507
07	CDS E-0162
08	CDS E-0322
09	CDS E-0509
10	CDS E-0321
11	CDS E-0508
12	CDS E-0163
13	CDS E-0507
14	CDS E-0162
15	CDS E-0322
16	CDS E-0509
17	CDS E-0321
18	CDS E-0508
19	CDS E-0163
20	CDS E-0507
21	CDS E-0162
22	CDS E-0322
23	CDS E-0509
24	CDS E-0321
25	CDS E-0508
26	CDS E-0163
27	CDS E-0507
28	CDS E-0162
29	CDS E-0322
30	CDS E-0509

N1S (cont)

46	CDS E-0508
47	CDS E-0163
48	CDS E-0507
49	CDS E-0162
50	CDS E-0322
51	CDS E-0509
52	CDS E-0321
53	CDS E-0508
54	CDS E-0163
55	CDS E-0507
56	CDS E-0162
57	CDS E-0322
58	CDS E-0509
59	CDS E-0321
60	CDS E-0508
61	CDS E-0163
62	CDS E-0507
63	CDS E-0162
64	CDS E-0322
65	CDS E-0509
66	CDS E-0321
67	CDS E-0508
68	CDS E-0163
69	CDS E-0507
70	CDS E-0162
71	CDS E-0322
72	CDS E-0509
73	CDS E-0321
74	CDS E-0508
75	CDS E-0163
76	CDS E-0507

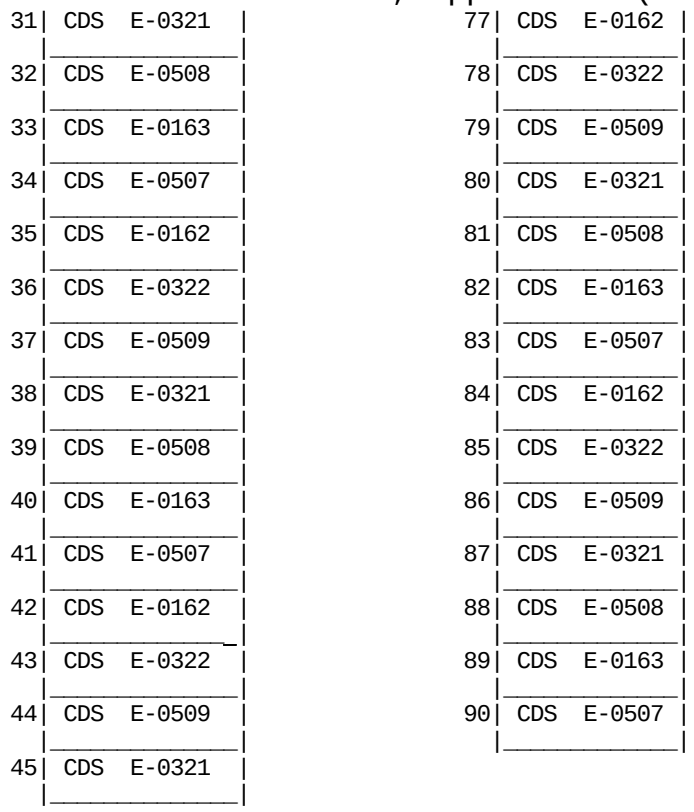


Figure A2.2.13. Fixed Area Measurement Assignment - HLM1A (cont)

	N1F					N1F (cont)			
00	CDS E-0664	CDS E-0665	CDS E-0666	CDS E-0667	46	CDS E-0753			
01	CDS E-0726		CDS E-0727		47	CDS E-0634		CDS E-0797	CDS E-0798
02	CDS E-0743				48	CDS E-0708	CDS E-0713	CDS E-0711	
03	CDS E-0656				49	CDS E-1010	CDS E-1011	CDS E-1012	CDS E-1013
04	CDS E-0793	CDS E-0686	CDS E-0687	CDS E-0695	50	CDS E-0758			
05	CDS E-0736		CDS E-0737		51	CDS E-0633		CDS E-0714	CDS E-0715
06	CDS E-0668	CDS E-0669			52	CDS E-0738			
07	CDS E-0674	CDS E-0676	CDS E-0677	CDS E-0679	53	CDS E-0753			
08	CDS E-0726		CDS E-0727		54	CDS E-0634		CDS E-0797	CDS E-0798
09	CDS E-0754				55	CDS E-0728		CDS E-0729	
10	CDS E-0799	CDS E-0800	CDS E-0801	CDS E-0802	56	CDS E-1010	CDS E-1011	CDS E-1012	CDS E-1013
11	CDS E-0793	CDS E-0686	CDS E-0687	CDS E-0695	57	CDS E-0657			CDS E-1006
12	CDS E-0749				58	CDS E-0683	CDS E-0684	CDS E-0685	
13	CDS E-0668	CDS E-0669			59	CDS E-0738			
14	CDS E-0674	CDS E-0676	CDS E-0677	CDS E-0679	60	CDS E-0671			
15	CDS E-0740				61	CDS E-0696	CDS E-0700		
16	CDS E-0754				62	CDS E-0728		CDS E-0729	
17	CDS E-0799	CDS E-0800	CDS E-0801	CDS E-0802	63	CDS E-0755			
18	CDS E-0730		CDS E-0731		64	CDS E-0803	CDS E-0804	CDS E-0805	CDS E-0806
19	CDS E-0749				65	CDS E-0683	CDS E-0684	CDS E-0685	
20	CDS E-0659				66	CDS E-0750			
21	CDS E-0689	CDS E-0690			67	CDS E-0671			
22	CDS E-0740				68	CDS E-0696	CDS E-0700		
23	CDS E-0644	CDS E-0655	CDS E-0658	CDS E-0705	69	CDS E-0741			
24	CDS E-0702			CDS E-0703	70	CDS E-0755			
25	CDS E-0730		CDS E-0731		71	CDS E-0803	CDS E-0804	CDS E-0805	CDS E-0806
26	CDS E-0756				72	CDS E-0732		CDS E-0733	
27	CDS E-0807	CDS E-0829	CDS E-0789	CDS E-0791	73	CDS E-0750			
28	CDS E-0689	CDS E-0690			74	CDS E-0660			
29	CDS E-0751				75	CDS E-0722		CDS E-0723	
30	CDS E-0644	CDS E-0655	CDS E-0658	CDS E-0705	76	CDS E-0741			
31	CDS E-0702			CDS E-0703	77	CDS E-0653			
32	CDS E-0742				78	CDS E-0706			CDS E-0707
33	CDS E-0756				79	CDS E-0732		CDS E-0733	
34	CDS E-0807	CDS E-0829	CDS E-0789	CDS E-0791	80	CDS E-0757			
35	CDS E-0734		CDS E-0735		81	CDS E-0638		CDS E-0636	
36	CDS E-0751				82	CDS E-0722		CDS E-0723	
37	CDS E-1010	CDS E-1011	CDS E-1012	CDS E-1013	83	CDS E-0752			
38	CDS E-0724		CDS E-0725		84	CDS E-0664	CDS E-0665	CDS E-0666	CDS E-0667
39	CDS E-0742				85	CDS E-0706			CDS E-0707
40	CDS E-0654			CDS E-1005	86	CDS E-0743			
41	CDS E-0708	CDS E-0713	CDS E-0711		87	CDS E-0757			
42	CDS E-0734		CDS E-0735		88	CDS E-0638		CDS E-0636	
43	CDS E-0758				89	CDS E-0736		CDS E-0737	
44	CDS E-0633		CDS E-0714	CDS E-0715	90	CDS E-0752			
45	CDS E-0724		CDS E-0725						

Figure A2.2.14. Fixed Area Measurement Assignment - HLM1B

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

N1S		N1S (cont)	
00	CDS E-0662	46	CDS E-1008
01	CDS E-0822	47	CDS E-0663
02	CDS E-1009	48	CDS E-1007
03	CDS E-0821	49	CDS E-0662
04	CDS E-1008	50	CDS E-0822
05	CDS E-0663	51	CDS E-1009
06	CDS E-1007	52	CDS E-0821
07	CDS E-0662	53	CDS E-1008
08	CDS E-0822	54	CDS E-0663
09	CDS E-1009	55	CDS E-1007
10	CDS E-0821	56	CDS E-0662
11	CDS E-1008	57	CDS E-0822
12	CDS E-0663	58	CDS E-1009
13	CDS E-1007	59	CDS E-0821
14	CDS E-0662	60	CDS E-1008
15	CDS E-0822	61	CDS E-0663
16	CDS E-1009	62	CDS E-1007
17	CDS E-0821	63	CDS E-0662
18	CDS E-1008	64	CDS E-0822
19	CDS E-0663	65	CDS E-1009
20	CDS E-1007	66	CDS E-0821
21	CDS E-0662	67	CDS E-1008
22	CDS E-0822	68	CDS E-0663
23	CDS E-1009	69	CDS E-1007
24	CDS E-0821	70	CDS E-0662
25	CDS E-1008	71	CDS E-0822
26	CDS E-0663	72	CDS E-1009
27	CDS E-1007	73	CDS E-0821
28	CDS E-0662	74	CDS E-1008
29	CDS E-0822	75	CDS E-0663
30	CDS E-1009	76	CDS E-1007

31	CDS	E-0821	
32	CDS	E-1008	
33	CDS	E-0663	
34	CDS	E-1007	
35	CDS	E-0662	
36	CDS	E-0822	
37	CDS	E-1009	
38	CDS	E-0821	
39	CDS	E-1008	
40	CDS	E-0663	
41	CDS	E-1007	
42	CDS	E-0662	
43	CDS	E-0822	
44	CDS	E-1009	
45	CDS	E-0821	

77	CDS	E-0662	
78	CDS	E-0822	
79	CDS	E-1009	
80	CDS	E-0821	
81	CDS	E-1008	
82	CDS	E-0663	
83	CDS	E-1007	
84	CDS	E-0662	
85	CDS	E-0822	
86	CDS	E-1009	
87	CDS	E-0821	
88	CDS	E-1008	
89	CDS	E-0663	
90	CDS	E-1007	

Figure A2.2.14. Fixed Area Measurement Assignment - HLM1B (cont)

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

S1S

00	DMS	E-1650
01	DMS	E-1650
02	DMS	E-1650
03	RFS	E-0023
04	EUV	E-1680
05	PPS	E-0086
06	PPS	E-0086

S2S

00	PPS	E-0080
01	RFS	E-0024
02	PPS	E-0082
03	RFS	E-0024
04	PPS	E-0080
05	RFS	E-0024
06	PPS	E-0082

T1S

00	CDS	E-0423
01	RPM	E-1613
02	CDS	E-0423
03	RFS	E-0032
04	RPM	E-1602
05	RPM	E-1610
06	RPM	E-1615
07	CDS	E-0423
08	CDS	E-1109
09	RFS	E-0034
10	RPM	E-1619
11	CDS	E-1110
12	CDS	E-0423

T2S

00	CDS	E-0424
01	CDS	E-0424
02	CDS	E-0424
03	DMS	E-1652
04	DMS	E-1652
05	DMS	E-1652
06	CDS	E-0424
07	CDS	E-0424
08	CDS	E-0424
09	DMS	E-1652
10	DMS	E-1652
11	DMS	E-1652
12	CDS	E-0424

N1D

00	RFS	E-0043	RFS	E-0028
01	CDS	E-0384	CDS	E-0385
02	CDS	E-0379		
03	MAG	S-1844		
04	CDS	E-0413	CDS	E-0414
05	CDS	E-0373	CDS	E-0374
06	PPS	E-0078	PPS	E-0089
07	CDS	E-1100	CDS	E-1101
08	CDS	E-0388	CDS	E-0389
09	STRU	E-0000	STRU	E-0002
10	MDS	E-0055	MDS	E-0056
11	CDS	E-0415		
12	MAG	E-1860	MAG	E-1862
13	RPM	E-1596	RPM	E-1598
14	CDS	E-1104	CDS	E-1105
15	RFS	E-0032	RFS	E-0034
16	DEV	E-1645	MDS	E-0058
17	RFS	E-0032	RFS	E-0034
18	CDS	E-0388	CDS	E-0389
19	CDS	E-0381		
20	AACS	E-1486	SXA	E-1660
21	CDS	E-0415		
22	CDS	E-0376		
23	PWS	E-1675	DDS	E-1740

N1D (cont)

30	EUV	E-1681	EUV	E-1680
31	CDS	E-0402	CDS	E-0408
32	DEV	E-1645	MDS	E-0058#
33	CDS	E-0419	CDS	E-0425
34	DEV	E-1645	MDS	E-0058#
35	CDS	E-0393	CDS	E-0395
36	RFS	E-0030	RFS	E-0031
37	RFS	E-0020	RFS	E-0053
38	CDS	E-0382	CDS	E-0383
39	CDS	E-0378		
40	MAG	S-1846		
41	CDS	E-0402	CDS	E-0408
42	CDS	E-0371	CDS	E-0372
43	PPS	E-0065	PPS	E-0069
44	RPM	E-1588	RPM	E-1591
45	CDS	E-0386	CDS	E-0387
46	CDS	E-0421	CDS	E-0422
47	AACS	E-1486	SXA	E-1660
48	CDS	E-0417	CDS	E-0418
49	CDS	E-1109	CDS	E-1110
50	CDS	E-0428	CDS	E-0429
51	CDS	E-1102	CDS	E-1103
52	RFS	E-0030	RFS	E-0031
53	DEV	E-1638	DEV	E-1639

N1D (cont)

60	EPD	E-1691	EPD	E-1690
61	CDS	E-1102	CDS	E-1103
62	CDS	E-0390	CDS	E-0369
63	STRU	E-0004	STRU	E-0006
64	RFS	E-0020	RFS	E-0053
65	CDS	E-0416		
66	CDS	E-0398	CDS	E-0399
67	RPM	E-1600	RPM	E-1603
68	CDS	E-1106	CDS	E-1108
69	DEV	E-1638	DEV	E-1639
70	CDS	E-0365	CDS	E-0366
71	DEV	E-1638	DEV	E-1639
72	CDS	E-0390	CDS	E-0369
73	RFS	E-0043	RFS	E-0028
74	MDS	E-0055	MDS	E-0056
75	CDS	E-0416		
76	CDS	E-0377		
77	MAG	S-1848		
78	CDS	E-1106	CDS	E-1108
79	CDS	E-0370		
80	PPS	E-0073	PPS	E-0096
81	RPM	E-1585	RPM	E-1586
82	CDS	E-0384	CDS	E-0385
83	CDS	E-0400		

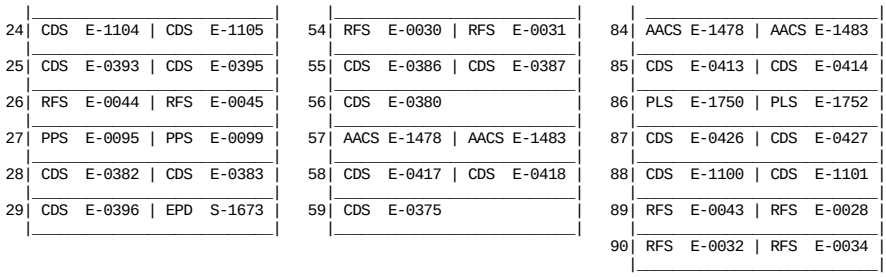


Figure A2.2.15. Fixed Area Measurement Assignment - LLM1A

*Includes PPS/MDS/CDS

#These deck slots to be "nulled" on Ground Decom Tables

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

S1S

00	DMS	E-1651
01	DMS	E-1651
02	DMS	E-1651
03	RFS	E-0022
04	HIC	E-1720
05	PPS	E-0087
06	RFS	E-0026

S2S

00	RFS	E-0025
01	PPS	E-0081
02	RFS	E-0025
03	PPS	E-0083
04	RFS	E-0025
05	PPS	E-0081
06	RFS	E-0025

T1S

00	RPM	E-1587
01	RPM	E-1616
02	PPS	E-0087
03	RPM	E-1601
04	PPS	E-0088
05	CDS	E-1130
06	RPM	E-1609
07	RPM	E-1589
08	CDS	E-1129
09	CDS	E-0923
10	CDS	E-0923
11	CDS	E-0923
12	PPS	E-0087

T2S

00	RPM	E-1617
01	STRU	E-0016
02	DMS	E-1653
03	CDS	E-0924
04	CDS	E-0924
05	CDS	E-0924
06	RFS	E-0033
07	RPM	E-1614
08	RPM	E-1608
09	CDS	E-0924
10	CDS	E-0924
11	CDS	E-0924
12	DMS	E-1653

N1D

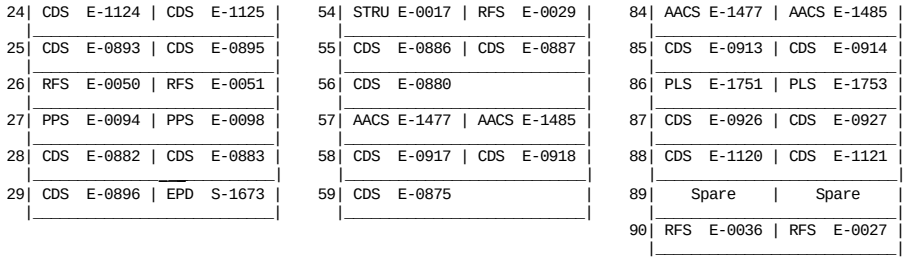
00	Spare		Spare	
01	CDS	E-0884	CDS	E-0885
02	CDS	E-0879		
03	MAG	S-1844		
04	CDS	E-0913	CDS	E-0914
05	CDS	E-0873	CDS	E-0874
06	Spare		Spare	
07	CDS	E-1120	CDS	E-1121
08	CDS	E-0888	CDS	E-0889
09	STRU	E-0001	STRU	E-0003
10	MDS	E-0059	MDS	E-0060
11	CDS	E-0915		
12	MAG	E-1861	MAG	E-1863
13	RPM	E-1597	RPM	E-1599
14	CDS	E-1124	CDS	E-1125
15	RFS	E-0036	RFS	E-0027
16	DEV	E-1646	MDS	E-0062
17	RFS	E-0036	RFS	E-0027
18	CDS	E-0888	CDS	E-0889
19	CDS	E-0881		
20	AACS	E-1487	AACS	E-1472
21	CDS	E-0915		
22	CDS	E-0876		
23	PWS	E-1676	DEV	E-1636

N1D (cont)

30	HIC	E-1722	Spare	
31	CDS	E-0902	CDS	E-0908
32	DEV	E-1646	MDS	E-0062#
33	CDS	E-0919	CDS	E-0925
34	DEV	E-1646	MDS	E-0062#
35	CDS	E-0893	CDS	E-0895
36	STRU	E-0017	RFS	E-0029
37	RFS	E-0052	RFS	E-0021
38	CDS	E-0882	CDS	E-0883
39	CDS	E-0878		
40	MAG	S-1846		
41	CDS	E-0902	CDS	E-0908
42	CDS	E-0871	CDS	E-0872
43	PPS	E-0066	PPS	E-0070
44	RPM	E-1590	RPM	E-1595
45	CDS	E-0886	CDS	E-0887
46	CDS	E-0921	CDS	E-0922
47	AACS	E-1487	AACS	E-1472
48	CDS	E-0917	CDS	E-0918
49	CDS	E-1129	CDS	E-1130
50	CDS	E-0928	CDS	E-0929
51	CDS	E-1122	CDS	E-1123
52	STRU	E-0017	RFS	E-0029
53	DEV	E-1637	DEV	E-1640

N1D (cont)

60	EPD	E-1693	EPD	E-1692
61	CDS	E-1122	CDS	E-1123
62	CDS	E-0890	CDS	E-0869
63	STRU	E-0005	STRU	E-0007
64	RFS	E-0052	RFS	E-0021
65	CDS	E-0916		
66	CDS	E-0898	CDS	E-0899
67	RPM	E-1604	RPM	E-1605
68	CDS	E-1126	CDS	E-1128
69	DEV	E-1637	DEV	E-1640
70	CDS	E-0865	CDS	E-0866
71	DEV	E-1637	DEV	E-1640
72	CDS	E-0890	CDS	E-0869
73	Spare		Spare	
74	MDS	E-0059	MDS	E-0060
75	CDS	E-0916		
76	CDS	E-0877		
77	MAG	S-1848		
78	CDS	E-1126	CDS	E-1128
79	CDS	E-0870		
80	PPS	E-0075	PPS	E-0100
81	RPM	E-1587	RPM	E-1589
82	CDS	E-0884	CDS	E-0885
83	CDS	E-0900		



*Includes MDS/PPS/CDS

Figure A2.2.16. Fixed Area Measurement Assignment - LLM1B

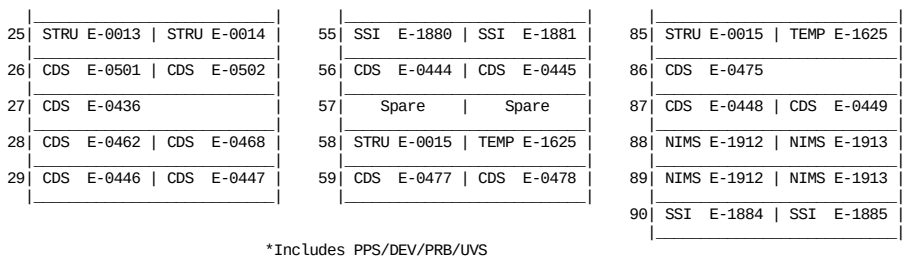
#These deck slots to be "nulled" on Grond Decom Tables

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

N1D			
00	CDS E-0501	CDS E-0502	
01	CDS E-0473	CDS E-0474	
02	CDS E-0442	CDS E-0443	
03	Spare	Spare	
04	STRU E-0011	STRU E-0012	
05	SCAS E-1945	SCAS E-1947	
06	CDS E-0448	CDS E-0449	
07	CDS E-0439		
08	CDS E-0458	CDS E-0459	
09	STRU E-0008	CDS E-0503	
10	CDS E-0433	CDS E-0434	
11	UVS E-1790	CDS E-1136	
12	CDS E-0442	CDS E-0443	
13	CDS E-0501	CDS E-0502	
14	NIMS E-1916	CDS E-0504	
15	NIMS E-1914	NIMS E-1915	
16	NIMS E-1912	NIMS E-1913	
17	SSI E-1882	SSI E-1883	
18	SSI E-1882	SSI E-1883	
19	CDS E-0446	CDS E-0447	
20	Spare	Spare	
21	PPR E-1715	PPR E-1716	
22	CDS E-0475		
23	AACS E-1473	AACS E-1475	
24	CDS E-0441		

N1D (cont)			
30	AACS E-1479	AACS E-1482	
31	STRU E-0011	STRU E-0012	
32	CDS E-0477	CDS E-0478	
33	NIMS E-1916	CDS E-0504	
34	NIMS E-1910	NIMS E-1911	
35	NIMS E-1910	NIMS E-1911	
36	SSI E-1882	SSI E-1883	
37	Spare	Spare	
38	CDS E-0462	CDS E-0468	
39	CDS E-0501	CDS E-0502	
40	DEV E-1647	PPS E-0067	
41	STRU E-0009	STRU E-0010	
42	PPS E-0074	PPS E-0076	
43	NIMS S-1929	NIMS S-1930	
44	CDS E-0438		
45	CDS E-0456	CDS E-0479	
46	PPS E-0092	PPS E-0093	
47	CDS E-0431	CDS E-0432	
48	PPR E-1715	PPR E-1716	
49	CDS E-0476		
50	CDS E-0453	CDS E-0455	
51	NIMS E-1914	NIMS E-1915	
52	CDS E-0501	CDS E-0502	
53	NIMS E-1910	NIMS E-1911	
54	SSI E-1880	SSI E-1881	

N1D (cont)			
60	CDS E-0453	CDS E-0455	
61	CDS E-0440		
62	CDS E-0460		
63	NIMS S-1924	NIMS S-1925	
64	CDS E-0435		
65	CDS E-0501	CDS E-0502	
66	CDS E-0444	CDS E-0445	
67	AACS E-1474	AACS E-1476	
68	STRU E-0009	STRU E-0010	
69	NIMS E-1916	CDS E-0504	
70	NIMS E-1914	NIMS E-1915	
71	SSI E-1884	SSI E-1885	
72	SSI E-1884	SSI E-1885	
73	SSI E-1880	SSI E-1881	
74	Spare	Spare	
75	UVS E-1790	CDS E-1136	
76	CDS E-0476		
77	AACS E-1480	AACS E-1481	
78	CDS E-0501	CDS E-0502	
79	PPS E-0071	PPS E-0072	
80	NIMS S-1926	NIMS S-1927	
81	CDS E-0437		
82	CDS E-0473	CDS E-0474	
83	PPS E-0077	PPS E-0079	
84	CDS E-0430		



*Includes PPS/DEV/PRB/UVS

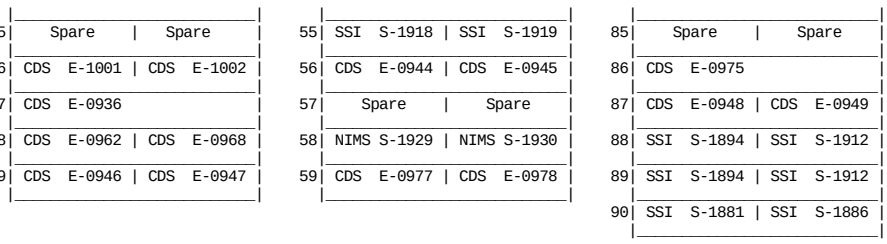
Figure A2.2.17. Fixed Area Measurement Assignment - LLM2A

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

N1D			
00	CDS E-1001	CDS E-1002	
01	CDS E-0973	CDS E-0974	
02	CDS E-0942	CDS E-0943	
03	Spare	Spare	
04	NIMS S-1926	NIMS S-1927	
05	NIMS S-1929	NIMS S-1930	
06	CDS E-0948	CDS E-0949	
07	CDS E-0939		
08	CDS E-0958	CDS E-0959	
09	Spare	CDS E-1003	
10	CDS E-0933	CDS E-0934	
11	Spare	Spare	
12	CDS E-0942	CDS E-0943	
13	CDS E-1001	CDS E-1002	
14	Spare	CDS E-1004	
15	SSI S-1841	SSI S-1842	
16	SSI S-1894	SSI S-1912	
17	SSI S-1915	SSI S-1840	
18	SSI S-1915	SSI S-1840	
19	CDS E-0946	CDS E-0947	
20	Spare	Spare	
21	Spare	Spare	
22	CDS E-0975		
23	NIMS S-1924	NIMS S-1925	
24	CDS E-0941		

N1D (cont)			
30	Spare	Spare	
31	Spare	Spare	
32	CDS E-0977	CDS E-0978	
33	Spare	CDS E-1004	
34	SSI S-1888	SSI S-1890	
35	SSI S-1888	SSI S-1890	
36	SSI S-1915	SSI S-1840	
37	Spare	Spare	
38	CDS E-0962	CDS E-0968	
39	CDS E-1001	CDS E-1002	
40	NIMS S-1929	NIMS S-1930	
41	NIMS S-1924	NIMS S-1925	
42	NIMS S-1926	NIMS S-1927	
43	Spare	Spare	
44	CDS E-0938		
45	CDS E-0956	CDS E-0979	
46	Spare	Spare	
47	CDS E-0931	CDS E-0932	
48	Spare	Spare	
49	CDS E-0976		
50	CDS E-0953	CDS E-0955	
51	SSI S-1841	SSI S-1842	
52	CDS E-1001	CDS E-1002	
53	SSI S-1888	SSI S-1890	
54	SSI S-1918	SSI S-1919	

N1D (cont)			
60	CDS E-0953	CDS E-0955	
61	CDS E-0940		
62	CDS E-0960		
63	Spare	Spare	
64	CDS E-0935		
65	CDS E-1001	CDS E-1002	
66	CDS E-0944	CDS E-0945	
67	Spare	Spare	
68	Spare	Spare	
69	Spare	CDS E-1004	
70	SSI S-1841	SSI S-1842	
71	SSI S-1881	SSI S-1886	
72	SSI S-1881	SSI S-1886	
73	SSI S-1918	SSI S-1919	
74	Spare	Spare	
75	Spare	Spare	
76	CDS E-0976		
77	NIMS S-1926	NIMS S-1927	
78	CDS E-1001	CDS E-1002	
79	NIMS S-1924	NIMS S-1925	
80	Spare	Spare	
81	CDS E-0937		
82	CDS E-0973	CDS E-0974	
83	Spare	Spare	
84	CDS E-0930		



*Includes PPS/DEV/PRB

Figure A2.2.18. Fixed Area Measurement Assignment - LLM2B

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

T1D	
00	AACS E-1226
01	AACS E-1284
02	AACS E-1248
03	AACS E-1212
04	AACS E-1219
05	AACS E-1232
06	AACS E-1220
07	AACS E-1233
08	AACS E-1208
09	AACS E-1202
10	AACS E-1264
11	AACS E-1209
12	AACS E-1254

T2D	
00	AACS E-1227
01	AACS E-1431
02	AACS E-1211
03	AACS E-1210
04	AACS E-1217
05	AACS E-1218
06	AACS E-1204
07	AACS E-1206
08	AACS E-1293
09	AACS E-1294
10	AACS E-1278
11	AACS E-1201
12	AACS E-1419

T3D	
00	AACS E-1370
01	AACS E-1247
02	AACS E-1267
03	AACS E-1255
04	AACS E-1230
05	AACS E-1231
06	AACS E-1205
07	AACS E-1207
08	AACS E-1215
09	AACS E-1282
10	AACS E-1336
11	AACS E-1338
12	AACS E-1420

N1D	
00	AACS E-1332
01	AACS E-1333
02	AACS E-1257
03	AACS E-1266
04	AACS E-1405
05	AACS E-1328
06	AACS E-1329
07	AACS E-1295
08	AACS E-1289
09	AACS E-1406
10	AACS E-1222
11	AACS E-1249
12	AACS E-1250
13	AACS E-1251
14	AACS E-1252
15	AACS E-1253
16	AACS E-1386
17	AACS E-1390
18	AACS E-1391
19	AACS E-1417
20	AACS E-1418
21	AACS E-1421
22	AACS E-1343
23	AACS E-1210
24	AACS E-1341

N1D (cont)	
30	AACS E-1279
31	AACS E-1213
32	AACS E-1203
33	AACS E-1405
34	AACS E-1392
35	AACS E-1270
36	AACS E-1289
37	AACS E-1342
38	AACS E-1406
39	AACS E-1374
40	AACS E-1375
41	AACS E-1376
42	AACS E-1406
43	AACS E-1276
44	AACS E-1389
45	AACS E-1433
46	AACS E-1430
47	AACS E-1433
48	AACS E-1444
49	AACS E-1256
50	AACS E-1340
51	AACS E-1319
52	AACS E-1371
53	AACS E-1372
54	AACS E-1373

N1D (cont)	
60	AACS E-1244
61	AACS E-1245
62	AACS E-1405
63	AACS E-1246
64	AACS E-1387
65	AACS E-1388
66	AACS E-1405
67	AACS E-1289
68	AACS E-1432
69	AACS E-1433
70	AACS E-1225
71	AACS E-1406
72	AACS E-1337
73	AACS E-1438
74	AACS E-1339
75	AACS E-1305
76	AACS E-1296
77	AACS E-1297
78	AACS E-1298
79	AACS E-1299
80	AACS E-1393
81	AACS E-1277
82	AACS E-1330
83	AACS E-1331
84	AACS E-1288

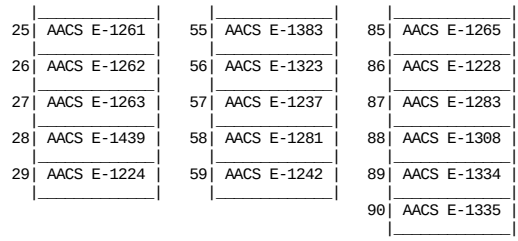


Figure A2.2.19. Fixed Area Measurement Assignment - AACS

Unmarked bars = ECR 35607

GLL-3-280 Rev. D, Appendix D (**PHASE 2**)

N2D		N2D (cont)		N2D (cont)		Z1D		Z2D		Z1S		Z2S	
00	AACS E-1303	30	AACS E-1304	60	AACS E-1304	00	AACS E-1396	00	AACS E-1397	00	AACS E-1394	00	AACS E-1395
01	AACS E-1304	31	AACS E-1304	61	AACS E-1304								
02	AACS E-1304	32	AACS E-1304	62	AACS E-1304								
03	AACS E-1304	33	AACS E-1304	63	AACS E-1304								
04	AACS E-1304	34	AACS E-1304	64	AACS E-1304								
05	AACS E-1304	35	AACS E-1304	65	AACS E-1304								
06	AACS E-1304	36	AACS E-1304	66	AACS E-1304								
07	AACS E-1304	37	AACS E-1304	67	AACS E-1304								
08	AACS E-1304	38	AACS E-1304	68	AACS E-1304								
09	AACS E-1304	39	AACS E-1304	69	AACS E-1304								
10	AACS E-1304	40	AACS E-1304	70	AACS E-1304								
11	AACS E-1304	41	AACS E-1304	71	AACS E-1304								
12	AACS E-1304	42	AACS E-1304	72	AACS E-1304								
13	AACS E-1304	43	AACS E-1304	73	AACS E-1304								
14	AACS E-1304	44	AACS E-1304	74	AACS E-1304								
15	AACS E-1304	45	AACS E-1304	75	AACS E-1304								
16	AACS E-1304	46	AACS E-1304	76	AACS E-1304								
17	AACS E-1304	47	AACS E-1304	77	AACS E-1304								
18	AACS E-1304	48	AACS E-1304	78	AACS E-1304								
19	AACS E-1304	49	AACS E-1304	79	AACS E-1304								
20	AACS E-1304	50	AACS E-1304	80	AACS E-1304								
21	AACS E-1304	51	AACS E-1304	81	AACS E-1304								
22	AACS E-1304	52	AACS E-1304	82	AACS E-1304								
23	AACS E-1304	53	AACS E-1304	83	AACS E-1304								
24	AACS E-1304	54	AACS E-1304	84	AACS E-1304								

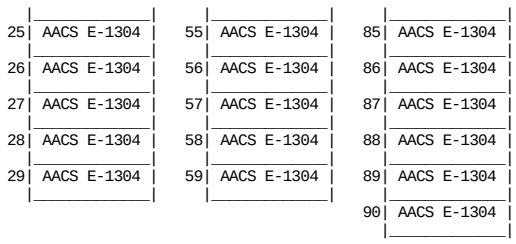


Figure A2.2.19. Fixed Area Measurement Assignment - AACS (cont)

A2.2.14.2.2 Variable Area Measurement Assignments.

The variable area measurements are grouped into packets, any of which may be placed into one or more engineering formats. The packets are listed in Table A2.2.8A, along with their associated measurements. The actual formats are shown in Figure A2.2.20, and described below.

a. Anomaly Format. The anomaly format shall provide telemetry for enhanced visibility into the spacecraft system for troubleshooting anomalies. This format shall be selectable either by ground command or by an onboard fault detection and correction routine. The format shall be assigned to commutation map identifier 0.

b. Launch Phase I Format (CDS load state). The Launch Phase I format shall provide telemetry from Launch to start of RPM pressurization. Note that GLL-3-120 defines the flight state for this format.

c. Launch Phase II Format (CDS load state). The launch phase II format shall provide telemetry during the RPM pressurization. Note that GLL-3-120 defines the flight state for this format.

d. Cruise/Encounter/Orbital Operations Format. The cruise/encounter/orbital operations format shall provide telemetry from the completion of the RPM pressurization through the end of mission, except for periods when maneuvers occur.

e. Launch Phase III/Maneuver/All Spin Format (CDS load state). The maneuver/all spin format shall provide telemetry during maneuvers and all spin operations, including TCM's. LRS (LPW) data will be available during these operations. Note that GLL-3-120 defines the flight state for this format.

Table A2.2.8A GLL Variable Telemetry Packet Listing

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
LOW LEVEL MODULE 1A	LLM 1A 01	RFS E-0024	RFS E-0042	RFS E-0031	RFS E-0034	RFS E-0038
	LLM 1A 02	PPS E-0078	PPS E-0086	PPS E-0080	PPS E-1635	PPS E-0090
	LLM 1A 03	spare	RFS E-0023	spare	spare	spare
	LLM 1A 04	RPM E-1585	RPM E-1586	RPM E-1588	RPM E-1591	PPS E-0065
	LLM 1A 05	RPM E-1591	PPS E-0065	RPM E-1585	RPM E-1586	RPM E-1588
	LLM 1A O6	RPM E-1596	RPM E-1598	RPM E-1600	RPM E-1602	RPM E-1603

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
LOW LEVEL MODULE 1B	LLM 1B 01	RFS E-0026	RFS E-0022	RFS E-0027	spare	spare
	LLM 1B 02	PPS E-0083	spare	spare	PPS E-1636	PPS E-0091
	LLM 1B 03	RFS E-0026	RPM E-1594	spare	spare	PPS E-0091
	LLM 1B 04	spare	spare	spare	RPM E-1594	spare
	LLM 1B 05	RPM E-1587	RPM E-1589	RPM E-1590	RPM E-1594	PPS E-0066
	LLM 1B 06	RPM E-1594	PPS E-0066	RPM E-1587	RPM E-1589	RPM E-1590
	LLM 1B O7	RPM E-1595	RPM E-1597	RPM E-1599	RPM E-1601	RPM E-1604

Table A2.2.8A GLL Variable Telemetry Packet Listing

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
LOW LEVEL MODULE 2A	LLM 2A 01	PPS E-0092	PPS E-0093	PPS E-0067	PPS E-1665	spare

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
LOW LEVEL MODULE 2B	LLM 2B 01	spare	spare	PPS E-0068	CTR E-1666	spare

Table A2.2.8A GLL Variable Telemetry Packet Listing (1200 Bps/Launch)

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
AACS	AACS 01	AACS E-1398		AACS E-1399		AACS E-1345
	AACS 02	AACS E-1400		AACS E-1401		AACS E-1346
	AACS 03	AACS E-1402		AACS E-1403		AACS E-1345
	AACS 04	AACS E-1404		AACS E-1240		AACS E-1346
	AACS 05	AACS E-1405		AACS E-1406		AACS E-1434
	AACS 06	AACS E-1221		AACS E-1234		AACS E-1383
	AACS 07	AACS E-1216		AACS E-1229		AACS E-1437
	AACS 08	AACS E-1226		AACS E-1227		AACS E-1283
	AACS 09	AACS E-1429		AACS E-1294		AACSE-1345
	AACS 10	AACS E-1415		AACS E-1416		AACS E-1290
	AACS 11	AACS E-1407		AACS E-1408		AACS E-1345
	AACS 12	AACS E-1409		AACS E-1410		AACS E-1346
	AACS 13	AACS E-1291		AACS E-1292		AACS E-1290
	AACS 14	AACS E-1426		AACS E-1354		AACS E-1434
	AACS 15	AACS E-1425		AACS E-1243		AACS E-1435
	AACS 16	AACS E-1417		AACS E-1418		AACS E-1346

Table A2.2.8A GLL Variable Telemetry Packet Listing (10/40 Bps)

Packet Source	Packet Name	Measurement #1	Measurement #2	Measurement #3	Measurement #4	Measurement #5
AACS	AACS 01	AACS E-1398		AACS E-1399		AACS E-1345
	AACS 02	AACS E-1400		AACS E-1401		AACS E-1346
	AACS 03	AACS E-1402		AACS E-1403		AACS E-1427
	AACS 04	AACS E-1404		AACS E-1240		AACS E-1345
	AACS 05	AACS E-1405		AACS E-1406		AACS E-1346
	AACS 06	AACS E-1221		AACS E-1234		AACS E-1383
	AACS 07	AACS E-1417		AACS E-1418		AACS E-1437
	AACS 08	AACS E-1226		AACS E-1227		AACS E-1283
	AACS 09	AACS E-1429		AACS E-1428		AACS E-1454
	AACS 10	AACS E-1200		AACS E-1215		AACS E-1454
	AACS 11	AACS E-1420		AACS E-1419		AACS E-1454
	AACS 12	AACS E-1423		AACS E-1424		AACS E-1290
	AACS 13	AACS E-1291		AACS E-1292		AACS E-1454
	AACS 14	AACS E-1208		AACS E-1354		AACS E-1290
	AACS 15	AACS E-1431		AACS E-1430		AACS E-1290
	AACS 16	AACS E-1303		AACS E-1225		AACS E-1290

Packet Position	1	2	3	4	5	6	7	8	9
Packet Name	LLM1A 01	LLM1A 02	LLM1B 01	spare	spare	AACS 04	AACS 05	AACS 10	AACS 15
Timing Position	A	C	A			N/A	N/A	N/A	N/A

Anomaly Format (Map 0)

Packet Name	LLM1A 01	LLM1A 03	LLM1B 02	LLM2A 01	LLM2B 01	AACS 10	AACS 06	AACS 03	AACS 05
Timing Position	A	C	A	A	A	N/A	N/A	N/A	N/A

Launch Phase I Format (Map 1, during launch phase)
(CDS load state, see GLL-3-120 for flight state)

Packet Name	LLM1A 04	LLM1A 05	LLM1A 06	LLM1B 05	LLM1B 06	LLM1B 07	spare	spare	spare
Timing Position	A	C	B	A	C	B			

Launch Phase II Format (Map 0, during launch phase)
(CDS load state, see GLL-3-120 for flight state)

Packet Name	LLM1A 01	LLM1A 02	LLM1B 01	AACS 11	AACS 12	AACS 13	AACS 14	AACS 15	AACS 05
Timing Position	A	C	A	N/A	N/A	N/A	N/A	N/A	N/A

Cruise/Encounter/Orbital Operations Format (Map 3)

Packet Name	LLM1A 01	LLM1A 03	LLM1B 03	LLM1B 04	LLM2A 01	LLM2B 01	AACS 03	AACS 04	AACS 10
Timing Position	A	C	A	C	A	A	N/A	N/A	N/A

Launch III/Maneuver/All Spin Format (Map 2)
(CDS load state, see GLL-3-120 for flight state)

Figure A2.2.20. GLL Variable Engineering Formats

A2.2.14.3 Digital and Software Measurements

Table A2.2.9 provides detailed data for each digital and software measurement. This data includes, subsystem, title, measurement engineering number, type (digital/software), width in bits, and the interpretation of individual bits.

Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Digital Bit Definitions

Bit(s)	Measurement	Contents
1	PPS 2.4 KHz inverter status A	0=main 1=standby
2	PPS PSU-1 pyro arm ind.	0=armed 1=safe
3	+X RTG isolation diode bypass	0=diode bypassed 1=diode unbypassed
4	PPS undervoltage trip ind - A	0=nominal voltage 1=undervoltage
5	RFS S-TWTA pwr output int - A	0=nominal pwr output 1=low pwr output
6	RFS X-exc pwr output int - A	0=nominal pwr output 1=low pwr output
7	RFS X-TWTA pwr output int - A	0=nominal pwr output 1=low pwr output
8	RFS S-exc pwr output int - A	0=nominal pwr output 1=low pwr output

|1|2|3|4|5|6|7|8| RFS/PPS status word 1 E-0018

Bit(s)	Measurement	Contents
1	PPS 2.4 KHz inverter status B	0=main 1=standby
2	PPS PSU-1 pyro unshort ind.	0=unshorted 1=shorted
3	-X RTG isolation diode bypass	0=diode bypassed 1=diode unbypassed
4	PPS undervoltage trip ind - B	0=nominal voltage 1=undervoltage
5	RFS S-TWTA pwr output int - B	0=nominal pwr output 1=low pwr output
6	RFS X-exc pwr output int - B	0=nominal pwr output 1=low pwr output
7	RFS X-TWTA pwr output int - B	0=nominal pwr output 1=low pwr output
8	RFS S-exc pwr output int - B	0=nominal pwr output 1=low pwr output

|1|2|3|4|5|6|7|8| RFS/PPS status word 2 E-0019

Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	X-band TWTA power	0=high power 1=low power
2	CS3 CW/CS4 CCW	0=off (HGA) 1=on (LGA-1 OR LGA-2)
3	S-band TWTA-2 on/off	0=off 1=on
4	X-band TWTA-1 on/off	0=off 1=on
5	two-way non-coherent	0=off 1=on
6	X-band exciter number	0=select 2 or X transmitters off 1=select 1
7	S-band ranging	0=on 1=off
8	receiver number	0=receiver 2 1=receiver 1

|1|2|3|4|5|6|7|8| RFS Status Word 1(A) E-0020

Bit(s)	Measurement	Contents
1	USO on/off	0=off 1=on
2	X-band ranging on/off	0=on 1=off
3	CS5 CCW	0=HGA (off) 1=LGA (on)
4	differential one-way ranging	0=off 1=on
5	S-band TWTA-1 on/off	0=off 1=on
6	S-band low/high power	0=high power 1=low power
7	S-band exciter number	0=select 2 or S exciters off 1=select 1
8	X-band TWTA-2 on/off	0=off 1=on

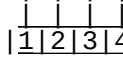
|1|2|3|4|5|6|7|8| RFS Status Word 2(B) E-0021

Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	X-band TWTA power	0=high power 1=low power
2	CS3 CW/CS4 CCW	0=off (HGA) 1=on (LGA-1 OR LGA-2)
3	S-band TWTA-2 on/off	0=off 1=on
4	X-band TWTA-1 on/off	0=off 1=on
5	two-way non-coherent	0=off 1=on
6	X-band exciter number	0=select 2 or X trans- mitters off 1=select 1
7	S-band ranging	0=on 1=off
8	receiver number	0=receiver 2 1=receiver 1

RFS Status Word 1(B) E-0052

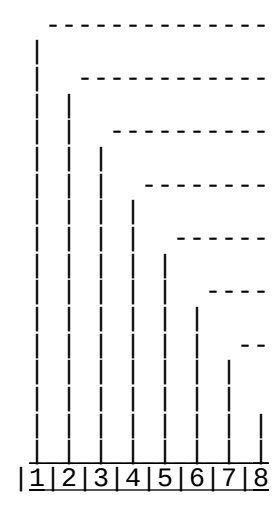
Bit(s)	Measurement	Contents
1	USO on/off	0=off 1=on
2	X-band ranging on/off	0=on 1=off
3	CS5 CCW	0=HGA (off) 1=LGA (on)
4	differential one-way ranging	0=off 1=on
5	S-band TWTA-1 on/off	0=off 1=on
6	S-band low/high power	0=high power 1=low power
7	S-band exciter number	0=select 2 or S exciters off 1=select 1
8	X-band TWTA-2 on/off	0=off 1=on



RFS Status Word 2(A) E-0053

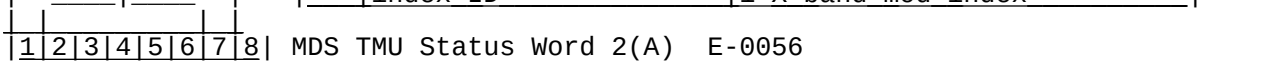
Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	X-band output 2	0=off 1=on
2	X-band output 1	0=off 1=on
3	X-band subcarrier frequency	0=low*/very high** 1=high
4	S-band data rate	0=low rate data 1=high rate data
5	S-band subcarrier frequency	0=low 1=high
6	S-band output 2	0=off 1=on
7	S-band output 1	0=off 1=on
8	TMU active unit indicator	0=TMU-B on 1=TMU-A on



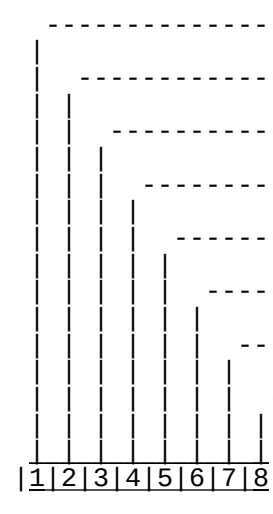
|1|2|3|4|5|6|7|8| MDS TMU Status Word 1(A) E-0055

Bit(s)	Measurement	Contents
1	CC select**/TDRS mode*	0=CC-1**/0=off* 1=CC-2**/1=on(no subcarrier)*
2-7	mod index	0=range 0-63 (22.22 mv per DN, 0=350 mv, 63=1750 mv)
8	X/S-band mod index ID	0=S-band mod index 1=X-band mod index



|1|2|3|4|5|6|7|8| MDS TMU Status Word 2(A) E-0056

Bit(s)	Measurement	Contents
1	X-band output 2	0=off 1=on
2	X-band output 1	0=off 1=on
3	X-band subcarrier frequency	0=low*/very high** 1=high
4	S-band data rate	0=low rate data 1=high rate data
5	S-band subcarrier frequency	0=low 1=high
6	S-band output 2	0=off 1=on
7	S-band output 1	0=off 1=on
8	TMU active unit indicator	0=TMU-B on 1=TMU-A on



|1|2|3|4|5|6|7|8| MDS TMU Status Word 1(B) E-0059

* Applies while on TMU-B
** Applies for TMU-A operation (CC-2 operation)

Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	CC select /TDRS mode TMU-A only/	0=CC-1/0=off* 1=CC-2/1=on (no subcarrier)*
2-7	mod index	0=range 0-63 (22.22 mv per DN, 0=350 mv, 63=1750 mv
8	X/S-band mod index ID	0=S-band mod index 1=X-band mod index

|1|2|3|4|5|6|7|8| MDS TMU Status Word 2(B) E-0060

Bit(s)	Measurement	Contents
1	CDS 4.8KHz test/A	0=inhibited 1=enabled
2	PSU-1A enable relays A status	0=enabled 1=disabled
3	spare	
4	PPS pyro amps 1A status (pyro events Mod 2)	0=even # of pyro events since BOM/POR 1=odd # of pyro events since BOM/POR
5	PPS discharge controller use ind.	0=not in use 1=in use
6	MDS TMU active unit ind	0=TMU-A active 1=TMU-B active
7	MDS CDU-A bit sync lock status	0=out of lock 1=in lock
8	MDS CDU-A subcarrier lock status	0=out of lock 1=in lock

|1|2|3|4|5|6|7|8| PPS/MDS/CDS status word 1 E-0065

Bit(s)	Measurement	Contents
1	CDS 4.8KHz test/B	0=inhibited 1=enabled
2	PSU-1B enable relays B status	0=enabled 1=disabled
3	spare	
4	PPS pyro amps 1B status (pyro events Mod 2)	0=even # of pyro events since BOM/POR 1=odd # of pyro events since BOM/POR
5	spare	
6	MDS CDU active unit ind	0=CDU-A active 1=CDU-B active
7	MDS CDU-B bit sync lock status	0=out of lock 1=in lock
8	MDS CDU-B subcarrier lock status	0=out of lock 1=in lock

|1|2|3|4|5|6|7|8| PPS/MDS/CDS status word 2 E-0066

* Applies while on TMU-B; for TMU-A operation, adjacent definitions apply.

Table A2.2.9. Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	PPS PSU-2A Probe enable relay status	0=enabled 1=disabled
2	DEV scan platform unlatch indicator	0=unlatched 1=stowed
3	PRB PPIU CCB inhibit 1 status	0=enabled 1=safe (see note 2)
4	PPS PSU-2 pyro arm ind.	0=armed 1=safe
5	PRB DCP descent power supply A status	0=off 1=on
6	PPS S/C separation enable relay status	0=enabled 1=disabled
7	S/C - IUS separation indicator A (see note 1 below)	0=separated 1=attached
8	PPS pyro amps 2A status (pyro events MOD 2)	0=even # of pyro events since BOM/POR 1=odd # of pyro events since BOM/POR

|1|2|3|4|5|6|7|8| PPS/DEV/PRB/UVS status word E-0067

Bit(s)	Measurement	Contents
1	PPS PSU-2B Probe enable relay status	0=enabled 1=disabled
2	DEV despun elctrnics unlatch indicator	0=unlatched 1=stowed
3	DEV spun-despun separation indicator	0=separated 1=attached
4	PPS PSU-2 pyro unshort ind.	0=unshorted 1=shorted
5	PRB DCP coast power supply status	0=off 1=on
6	PRB PPIU CCB inhibit 2 status	0=enabled 1=safe
7	S/C - IUS separation indicator B (see note 1 below)	0=separated 1=attached
8	PPS pyro amps 2B status (pyro events MOD 2)	0=even # of pyro events since BOM/POR 1=odd # of pyro events since BOM/POR

|1|2|3|4|5|6|7|8| PPS/DEV/PRB status word E-0068

Notes: 1) E-0067 (E-0068) bit 7 controls the S/C serial TLM data and clock sent to the STS/IUS "A" ("B") channel. Serial data and clock is enabled (inhibited) when bit 7 is a logical "1" ("0"). See Para graph 3.4.1.

2) UVS 30VDC power is also inhibited with the safe condition of PRB PPIU CCB inhibit 1 Status.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	LLM-2A MPLO	0=off	
		1=on	D
2	LLM-2A Memory Swap	0=off	
		1=on	D
3	LLM-2A CC/DC disable	0=off	
		1=on	D
4	LLM-2A bus select	0=BUS-2A	
		1=BUS-2B	D
5	LLM-2A bus adapter write protect	0=off	
		1=on	D
6	LLM-2A write protect 2000-2FFF/6000-6FFF	0=off	
		1=on	D
7	LLM-2A write protect 0000-1FFF/4000-5FFF	0=off	
		1=on	D
8	spare		

|1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 0-3 (MSB) E-0153

Bit(s)	Measurement	Contents	
1	LLM-2B MPLO	0=off	
		1=on	D
2	LLM-2B Memory Swap	0=off	
		1=on	D
3	LLM-2B CC/DC disable	0=off	
		1=on	D
4	LLM-2B bus select	0=BUS-2A	
		1=BUS-2B	
5	LLM-2B bus adapter write protect	0=off	
		1=on	D
6	LLM-2B write protect 2000-2FFF/6000-6FFF	0=off	
		1=on	D
7	LLM-2B write protect 0000-1FFF/4000-5FFF	0=off	
		1=on	D
8	spare		

|1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 0-3 (2SB) E-0153

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	RRH-2 bus select	0=BUS-2A	D
		1=BUS-2B	
2	RRH-1 bus select	0=BUS-2A	
		1=BUS-2B	D
3	PPR bus select	0=BUS-2A	D
		1=BUS-2B	
4	NIMS bus select	0=BUS-2A	D
		1=BUS-2B	
5	SSI bus select	0=BUS-2A	D
		1=BUS-2B	
6	UVS bus select	0=BUS-2A	D
		1=BUS-2B	
7-8	spare		

1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 0-3 (3SB) E-0153

1	CRC-2A BA write busy error status	0=no error	
		1=write attempt when busy	
2	CRC-2A BA write protect error status	0=no error	
		1=error	
3	HCD transfer error status	0=no error	
		1=error	
4	HCD POR status	0=no POR	
		1=one or more PORs	
5	BUS-2B POR status	0=no POR	
		1=one or more PORs	
6	BUS-2A POR status	0=no POR	
		1=one or more PORs	
7	CRC-2A BA bus parity error status	0=no error	
		1=one or more errors, any BA involved	
8	CRC-2A BA transaction parity error status	0=no error	
		1=one or more errors, CRC-2A BA involved	

1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 0-3 (LSB) E-0153 AND HLM1A DESPUN CRC BANK A E-0155

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	spare		
2	backup MUX control BIT-C	0=reset 1=set	 D
3	backup MUX control BIT-B	0=reset 1=set	 D
4	backup MUX control BIT-A	0=reset 1=set	 D
5	ADC-2A LLM select	0=LLM-2A 1=LLM-2B	 D
6	IUS/STS-2B low rate TLM select	0=LLM-2A 1=LLM-2B	D
7	IUS/STS-2A low rate TLM select	0=LLM-2A 1=LLM-2B	 D
8	CRC-2A critical enable master	0=off 1=on	

1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 4-6 (MSB) E-0154

Bit(s)	Measurement	Contents	
1-4	spare		
5	CRC-2B bus adapter write protect	0=off 1=on	 D
6	CRC-2B bus select	0=BUS-2A 1=BUS-2B	D
7	CRC-2A bus adapter write protect	0=off 1=on	 D
8	CRC-2A bus select	0=BUS-2A 1=BUS-2B	 D

1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 4-6 (2SB) E-0154

Bit(s)	Measurement	Contents	
1-2	spare		
3	DESPUN critical enable 5 (spare)	0=reset 1=set	D
4	DESPUN critical enable 4 (spare)	0=reset 1=set	
5	DESPUN critical enable 3 (spare)	0=reset 1=set	
6	DESPUN critical enable 2 (probe umbilical cable cutter enable)	0=reset (ENABLE RESET) 1=set (ENABLE)	D
7	DESPUN critical enable 1 (PPS spare)	0=reset (ENABLE RESET) 1=set (ENABLE)	D
8	DESPUN critical enable 0 (probe release enable)	0=reset (ENABLE RESET) 1=set (ENABLE)	D

1|2|3|4|5|6|7|8| HLM1A DESPUN CRC REGISTERS 4-6 (LSB) E-0154

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

For the bit definition of E-0155, see HLM1A DESPUN CRC REGISTERS 0-3 (LSB) E-0153. Their definitions are identical.

HLM1A DESPUN CRC REGISTERS 0-3 E-0155,

Bit(s)	Measurement	Contents		
1	HLM-1A MPLO	0=off		
		1=on		D
2	HLM-1A Memory Swap	0=off		
		1=on		D
3	HLM-1A write protect	0=off		
	5000-5FFF/D000-DFFF	1=on		D
4	HLM-1A write protect	0=off		
	4000-4FFF/C000-CFFF	1=on		D
5	HLM-1A write protect	0=off		
	3000-3FFF/B000-BFFF	1=on		D
6	HLM-1A write protect	0=off		
	2000-2FFF/A000-AFFF	1=on		D
7	HLM-1A write protect	0=off		
	1000-1FFF/9000-9FFF	1=on		D
8	HLM-1A write protect	0=off		
	0000-0FFF/8000-8FFF	1=on		D

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 0-3 (MSB) E-0156

1	LLM-1A MPLO	0=off		
		1=on		D
2	LLM-1A Memory Swap	0=off		
		1=on		D
3	LLM-1A CC/DC disable	0=off		
		1=on		D
4	LLM-1A bus select	0=BUS-1A		
		1=BUS-1B		D
5	LLM-1A bus adapter write	0=off		
	protect	1=on		D
6	LLM-1A write protect	0=off		
	2000-2FFF/6000-6FFF	1=on		D
7	LLM-1A write protect	0=off		
	0000-1FFF/4000-5FFF	1=on		D
8	spare			

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 0-3 (2SB) E-0156

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	BUM-1A BA-2B write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
2	BUM-1A BA-2B write protect 1000-17FF/5000-57FF	0=off 1=on	D
3	BUM-1A BA-2B write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
4	BUM-1A BA-2B write protect 0000-07FF/4000-47FF	0=off 1=on	D
5	BUM-1A BA-1A write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
6	BUM-1A BA-1A write protect 1000-17FF/5000-57FF	0=off 1=on	D
7	BUM-1A BA-1A write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
8	BUM-1A BA-1A write protect 0000-07FF/4000-47FF	0=off 1=on	D

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 0-3 (3SB) E-0156

Bit(s)	Measurement	Contents	
1	BUM-1A TLM control BA select	0=BA-1A 1=BA-2B	D
2	Golay-1A bus select	0=BUS-1A 1=BUS-1B	D
3	BUM-1A BA-2B bus select	0=BUS-1A 1=BUS-1B	D
4	BUM-1A BA-1A bus select	0=BUS-1A 1=BUS-1B	D
5	BUM-1A memory swap	0=off 1=on	D
6	BUM-1A write protect 3000-37FF/7000-77FF	0=off 1=on	D
7	BUM-1A write protect 2800-2FFF/6800-6FFF	0=off 1=on	D
8	BUM-1A write protect 2000-27FF/6000-67FF	0=off 1=on	D

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 0-3 (LSB) E-0156

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1-2	spare		
3	4.8 KHZ reference select	0=REF-1A	
		1=REF-1B	D
4-5	spare		
6	digital engineering serial-binary select	0=LLM-1A	
		1=LLM-1B	D
7	digital engineering timing chain select	0=TC-1A	
		1=TC-1B	D
8	CRC-1A critical enable master	0=off	
		1=on	

|1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 4-6 (MSB) E-0157

Bit(s)	Measurement	Contents	
1	HCD POR test control	0=off	
		1=on	D
2-4	spare		
5	HCD-1A override-3	0=on	
		1=off	
6	HCD-1A override-2	0=off	
		1=on	
7	HCD-1A override-1	0=off	
		1=on	
8	HCD-1B disable	0=off	
		1=on	

|1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 4-6 (2SB) E-0157

Bit(s)	Measurement	Contents	
1-2	spare		
3	spun critical enable 5 (spare)	0=reset	
		1=set	
4	spun critical enable 4 (RPN 2nd isolate and bypass enable)	0=reset (ENABLE RESET)	D
		1=set (ENABLE)	
5	spun critical enable 3 (AACS 400N engine enable)	0=reset (ENABLE)	
		1=set (DISABLE)	D
6	spun critical enable 2 (AACS memory B write protect)	0=reset	
		1=set	*
7	spun critical enable 1 (AACS memory A write protect)	0=reset	
		1=set	*
8	spun critical enable 0 (spare)	0=reset	
		1=set	

|1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK A REGISTERS 4-6 (LSB) E-0157

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

* Write Protect disabled when opposing string is set similarly;
Write Protect enabled when opposing string is set differently.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is HSB)

For the bit definition of E-0158, see HLM1A SPUN CRC STATUS WORD E-0168. Their definitions are identical.

HLM1A DESPUN CRC BANK A E-0158

Bit(s)	Measurement	Contents	
1	HLM-1B MPLO	0=off 1=on	D
2	HLM-1B memory swap	0=off 1=on	D
3	HLM-1B write protect 5000-5FFF/D000-DFFF	0=off 1=on	D
4	HLM-1B write protect 4000-4FFF/C000-CFFF	0=off 1=on	D
5	HLM-1B write protect 3000-3FFF/B000-BFFF	0=off 1=on	D
6	HLM-1B write protect 2000-2FFF/A000-AFFF	0=off 1=on	D
7	HLM-1B write protect 1000-1FFF/9000-9FFF	0=off 1=on	D
8	HLM-1B write protect 0000-0FFF/8000-8FFF	0=off 1=on	D

|1|2|3|4|5|6|7|8|

HLM1A SPUN CRC BANK B REGISTERS 0-3 (MSB) E-0159

Bit(s)	Measurement	Contents	
1	LLM-1B MPLO	0=off 1=on	D
3	LLM-1B memory swap	0=off 1=on	D
3	LLM-1B CC/DC disable	0=off 1=on	D
4	LLM-1B bus select	0=BUS-1A 1=BUS-1B	D
5	LLM-1B bus adapter write protect	0=off 1=on	D
6	LLM-1B write protect 2000-2FFF/6000-6FFF	0=off 1=on	D
7	LLM-1B write protect 0000-1FFF/4000-5FFF	0=off 1=on	D
8	spare		

|1|2|3|4|5|6|7|8|

HLM1A SPUN CRC BANK B REGISTERS 0-3 (2SB) E-0159

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	BUM-1B BA-2A write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
2	BUM-1B BA-2A write protect 1000-17FF/5000-57FF	0=off 1=on	D
3	BUM-1B BA-2A write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
4	BUM-1B BA-2A write protect 0000-07FF/4000-47FF	0=off 1=on	D
5	BUM-1B BA-1B write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
6	BUM-1B BA-1B write protect 1000-17FF/5000-57FF	0=off 1=on	D
7	BUM-1B BA-1B write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
8	BUM-1B BA-1B write protect 0000-07FF/4000-47FF	0=off 1=on	D

1|2|3|4|5|6|7|8 HLM1A SPUN CRC BANK B REGISTERS 0-3 (3SB) E-0159

Bit(s)	Measurement	Contents	
1	BUM-1B TLM control BA select	0=BA-1B 1=BA-2A	D
2	Golay-1B bus select	0=BUS-1A 1=BUS-1B	D
3	BUM-1B BA-2A bus select	0=BUS-1A 1=BUS-1B	D
4	BUM-1B BA-1B bus select	0=BUS-1A 1=BUS-1B	D
5	BUM-1B memory swap	0=off 1=on	D
6	BUM-1B write protect 3000-37FF/7000-77FF	0=off 1=on	D
7	BUM-1B write protect 2800-2FFF/6800-6FFF	0=off 1=on	D
8	BUM-1B write protect 2000-27FF/6000-67FF	0=off 1=on	D

1|2|3|4|5|6|7|8 HLM1A SPUN CRC BANK B REGISTERS 0-3 (LSB) E-0159

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	HIC/EUV bus select	0=BUS-1A	D
		1=BUS-1B	
2	DDS bus select	0=BUS-1A	D
		1=BUS-1B	
3	EPD bus select	0=BUS-1A	D
		1=BUS-1B	
4	PWS bus select	0=BUS-1A	D
		1=BUS-1B	
5	MAG bus select	0=BUS-1A	D
		1=BUS-1B	
6	PLS bus select	0=BUS-1A	D
		1=BUS-1B	
7	AACS-B bus select	0=BUS-1A	D
		1=BUS-1B	
8	AACS-A bus select	0=BUS-1A	
		1=BUS-1B	D

|1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK B REGISTERS 4-7 (MSB) E-0160

Bit(s)	Measurement	Contents	
1	DBUM-1B Memory Swap	0=off	
		1=on	D
2	DBUM-1A Memory Swap	0=off	
		1=on	D
3	spare		
4	HCD POR test select	0=PC-1A	
		1=PC-1B	D
5	timing chain manual	0=off	
	select control	1=on	D
6	timing chain manual	0=TC-1A	
	select	1=TC-1B	D
7	POR fault override	0=off	
	control	1=on	D
8	POR fault override	0=PC-1A	
	select	1=PC-1B	D

|1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK B REGISTERS 4-7 (2SB) E-0160

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	spare		
2-3	hi rate TLM mod TMU-1B select	00=LLM-1A (Note 1) 01=BUM-1A 10=LLM-1B 11=BUM-1B	
4	low rate TLM mod TMU-1B select	0=LLM-1A 1=LLM-1B	D
5	spare		
6-7	hi rate TLM mod TMU-1A select	00=LLM-1A (Note 2) 01=BUM-1A 10=LLM-1B 11=BUM-1B	
8	low rate TLM mod TMU-1A select	0=LLM-1A 1=LLM-1B	D

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK B REGISTERS 4-7 (3SB) E-0160

1	spare DBUM select	0=DBUM-1A 1=DBUM-1B	D
2	DBUM-1B bus select	0=BUS-1A 1=BUS-1B	D
3	DMS DBUM select	0=DBUM-1A 1=DBUM-1B	D
4	DBUM-1A bus select	0=BUS-1A 1=BUS-1B	D
5	CRC-1B bus adapter write protect	0=off 1=on	D
6	CRC-1B bus select	0=BUS-1A 1=BUS-1B	D
7	CRC-1A bus adapter write protect	0=off 1=on	D
8	CRC-1A bus select	0=BUS-1A 1=BUS-1B	D

1|2|3|4|5|6|7|8| HLM1A SPUN CRC BANK B REGISTERS 4-7 (LSB) E-0160

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Note 1 - The LLM's are the source only if both strings' CRC bit 3 are reset (logical 0). The A string (LLM or Bum) is the source only if both strings' CRC bit 2 are reset (logical 0).

Note 2 - The LLM's are the source only if both strings' CRC bit 7 are reset (logical 0). The B string (LLM or BUM) is the source only if both strings' CRC bit 6 are set (logical 1).

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-6	HCD-1A command message number	6 LSBs of cmd message sent to HCD-1A
7	HCD-1A start word bit error status	0=error-free start word 1=error in start word
8	HCD-1A message status	0=accepted 1=rejected

|1|2|3|4|5|6|7|8| HLM1A HCD COMMAND SUMMARY WORD E-0161

Bit(s)	Measurement	Contents
1-8	HCD-1A messages received and accepted counter	increments by one for each message accepted by HCD-1A (MOD 256)

|1|2|3|4|5|6|7|8| HLM1A MSG RCVD AND ACCEPTED COUNTER E-0162

Bit(s)	Measurement	Contents
1-8	HCD-1A messages received and rejected counter	increments by one for each message rejected by HCD-1A (MOD 256)

|1|2|3|4|5|6|7|8| HLM1A MSG RCVD AND RJCTD COUNTER E-0163

Bit(s)	Measurement	Contents
1-8	HCD-1A command frame errors detected counter	increments by one for each command frame detected with errors by HCD-1A (MOD 256)

|1|2|3|4|5|6|7|8| HLM1A CMD FRAME ERRORS DETECTED COUNTER E-0164

Bit(s)	Measurement	Contents
1-8	HCD-1A data frame errors corrected counter	increments by one for each data frame corrected by HCD-1A (MOD 256)

|1|2|3|4|5|6|7|8| HLM1A DATA FRAME ERRORS CORRECTED COUNTER E-0165

Bit(s)	Measurement	Contents
1-8	HCD-1A data frame errors uncorrectable counter	increments by one for each erroneous data frame uncorrectable by HCD-1A (MOD 256)

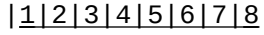
|1|2|3|4|5|6|7|8| HLM1A DATA FRAME ERRORS UNCORRECTABLE COUNTER E-0166

Bit(s)	Measurement	Contents
1-8	HCD-1A lock changes counter	increments by one for each lock change provided to HCD-1A (MOD 256)

|1|2|3|4|5|6|7|8| HLM1A LOCK CHANGES COUNTER E-0167

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

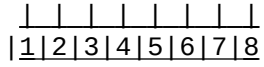
Bit(s)	Measurement	Contents
1	CRC-1A BA write busy error status	0=no error 1=write attempt when busy
2	CRC-1A BA write protect error status	0=no error 1=error
3	CRC-1A command block write attempt	0=no attempt 1=one or more attempts
4	CRC-1A power converter/ HCD POR status	0=no POR 1=one or more PORs
5	spare	
6	multiple frame CMD with zero data frames	0=no error 1=one or more errors
7	CRC-1A BA BUS parity error status	0=no error 1=one or more errors, any BA involved
8	CRC-1A BA transaction parity error status	0=no error 1=one or more errors, CRC-1A BA involved



HLM1A SPUN CRC STATUS WORD E-0168 AND
HLM1A SPUN CRC BANK A E-0158

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	BUS-1A overrun status	0=no overrun 1=overrun error, bus transaction in process at RTI
2	HLM-1A self-test failure status	0=pass 1=fail
3	HLM-1A keep-alive POR status	0=no KAPOR 1=one or more KAPORs with memory loss
4	HLM-1A POR status	0=no POR 1=one or more PORs, any power failure
5	HLM-1A microprocessor sync-idle status	0=in sync 1=out of sync (1802 vs BIS) /idle lockup
6	HLM-1A BA bus parity error status - despun mux	0=no error 1=one or more errors, any BA involved (DESPUN MUX)
7	HLM-1A BA bus parity error status	0=no error 1=one or more errors, any BA involved(BC or SPUN MUX)
8	HLM-1A BA transaction parity error status	0=no error 1=one or more errors, HLM-1A BA involved



HLM1A ERROR WORDS IOSL 0-1-2 (MSB) E-0169

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	HCD parity error status	0=no error 1=one or more parity errors from HCD to HLM-1A
2	HLM-1A microprocessor memory read parity error status	0=no error 1=one or more parity errors when memory read by processor
3	HLM-1A BA memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
4	HLM-1A bus controller memory read parity error status	0=no error 1=one or more parity errors when memory read by BC
5	HLM-1A microprocessor lockout status	0=no MPLO 1=MPLO
6	HLM-1A BA write protect error status	0=no error 1=write attempt by BA into protected memory
7	HLM-1A microprocessor write protect error status	0=no error 1=write attempt by processor into protected memory
8	HCD write protect error status	0=no error 1=write attempt by HCD into protected memory

|1|2|3|4|5|6|7|8| HLM1A ERROR WORDS IOSL 0-1-2 (2SB) E-0169

Bit(s)	Measurement	Contents
1-2	grounded spare	
3	PLL-1B timing chain select status	0=timing chain A 1=timing chain B
4	PLL-1A timing chain select status	0=timing chain A 1=timing chain B
5-6	grounded spare	
7	phase locked loop 1B POR status	0=no POR 1=one or more PORs
8	phase locked loop 1A POR status	0=no POR 1=one or more PORs

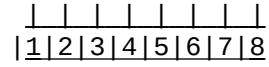
|1|2|3|4|5|6|7|8| HLM1A ERROR WORDS IOSL 0-1-2 (LSB) E-0169

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-3	spare	
4	BUM-1A POR status	0=no POR 1=one or more PORs
5	BUM-1A BA 2B bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
6	BUM-1A BA 2B transaction parity error status	0=no error 1=one or more parity errors involving BUM-1A's BA-2B
7	BUM-1A BA 1A bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
8	BUM-1A BA 1A transaction parity error status	0=no error 1=one or more parity errors involving BUM-1A's BA-1A

HLM1A BUM ERROR WORDS (MSB) E-0171

Bit(s)	Measurement	Contents
1	BUM-1A telemetry formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
2	BUM-1A telemetry sequencer memory read parity error status	0=no error 1=one or more parity errors when memory read by sequencer
3	BUM-1A BA-2B memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-2B
4	BUM-1A BA-1A memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-1A
5-6	spare	
7	BUM-1A BA-2B write protect error status	0=no error 1=write attempt by BA-2B into protected memory
8	BUM-1A BA-1A write protect error status	0=no error 1=write attempt by BA-1A into protected memory



HLM1A BUM ERROR WORDS (2SB) E-0171

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-3	spare	
4	BUM-1B POR status	0=no POR 1=one or more PORs
5	BUM-1B BA-2A bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
6	BUM-1B BA-2A transaction parity error status	0=no error 1=one or more parity errors involving BUM-1B's BA 2
7	BUM-1B BA-1B bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
8	BUM-1B BA-1B transaction parity error status	0=no error 1=one or more parity errors involving BUM-1B's BA 1

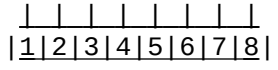
|1|2|3|4|5|6|7|8| HLM1A BUM ERROR WORDS (3SB) E-0171

1	BUM-1B telemetry formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
2	BUM-1B telemetry sequencer memory read parity error status	0=no error 1=one or more parity errors when memory read by sequencer
3	BUM-1B BA-2A memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-2A
4	BUM-1B BA-1B memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-1B
5-6	spare	
7	BUM-1B BA-2A write protect error status	0=no error 1=write attempt by BA-2A into protected memory
8	BUM-1B BA-1B write protect error status	0=no error 1=write attempt by BA-1B into protected memory

|1|2|3|4|5|6|7|8| HLM1A BUM ERROR WORDS (LSB) E-0171

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	DMS illegal command status	0=no illegal command 1=illegal cmd (not per DMS CMD dictionary)
2	DBUM-1A sequencer output memory read parity error status	0=no error 1=one or more parity errors when memory read by DBUM sequencer
3	DBUM-1A formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
4	DBUM-1A bus adapter memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
5	DMS tape direction status	0=forward 1=reverse
6	DBUM-1A POR status	0=no POR 1=one or more PORs
7	DBUM-1A bus adapter bus parity error status	0=no error 1=one or more parity errors involving any BA
8	DBUM-1A BA transaction parity error status	0=no error 1=one or more parity errors involving DBUM-1A BA



HLM1A DBUM ERROR WORDS (MSB) E-0172

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	DMS illegal command status	0=no illegal command 1=illegal cmd (not per DMS CMD dictionary)
2	DBUM-1B sequencer output memory read parity error status	0=no error 1=one or more parity errors when memory read by DBUM sequencer
3	DBUM-1B formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
4	DBUM-1B bus adapter memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
5	DMS tape direction status	0=forward 1=reverse
6	DBUM-1B POR status	0=no POR 1=one or more PORs
7	DBUM-1B bus adapter bus parity error status	0=no error 1=one or more parity errors involving any BA
8	DBUM-1B BA transaction parity error status	0=no error 1=one or more parity errors involving DBUM-1B BA

|1|2|3|4|5|6|7|8| HLM1A DBUM ERROR WORDS (LSB) E-0172

Bit(s)	Measurement	Contents
1	LLM-1A microprocessor lockout status	0=no MPLO 1=MPLO
2	LLM-1A self-test failure status	0=pass 1=fail
3	CC/DC in-process status	0=no cmd beginning execute 1=cmd beginning execute
4	LLM-1A POR status	0=no POR 1=one or more PORs, any power failure
5	LLM-1A microprocessor sync-idle error status	0=in sync 1=out of sync (1802 vs BIS) /idle lockup
6	CC/DC hardware buffer full status	0=empty 1=full
7	LLM-1A BA bus parity error status	0=no error 1=one or more errors, any BA involved
8	LLM-1A BA transaction parity error status	0=no error 1=one or more errors, LLM-1A BA involved

|1|2|3|4|5|6|7|8| LLM1A ERROR WORD-1 IOSL-0 E-0413

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	LLM-1A TLM port memory read parity error status	0=no error 1=one or more parity errors when memory read by TLM port
2	LLM-1A microprocessor memory read parity error status	0=no error 1=one or more parity errors when memory read by processor
3	LLM-1A BA memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
4	engineering control port memory read parity error status	0=no error 1=one or more parity errors when memory read by engr. control port
5	CC/DC error status	0=overwrite not attempted 1=attempt to load CC/DC H/W buffer when already full
6	LLM-1A BA write protect error status	0=no error 1=write attempt by BA into protected memory, or I/O selects
7	LLM-1A microprocessor write protect error status	0=no error 1=write attempt by processor into protected memory
8	engineering data port write protect error status	0=no error 1=write attempt by engr. data port into protected memory

|1|2|3|4|5|6|7|8| LLM1A ERROR WORD-2 IOSL-1 E-0414

Bit(s)	Measurement	Contents
1	DMS BOT/EOT status	0=BOT 1=EOT
2	DMS leader/tape status	0=on tape 1=on leader
3-8	tic count status (6 MSB)	6 MSBs of the 14 bit tic count

|1|2|3|4|5|6|7|8| LLM1A DMS TAPE POSITION ESTIMATE (MSB) E-0423

Bit(s)	Measurement	Contents
1-8	tic count status (8 LSB)	8 LSBs of the 14 bit tic count

|1|2|3|4|5|6|7|8| LLM1A DMS TAPE POSITION ESTIMATE (LSB) E-0424

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

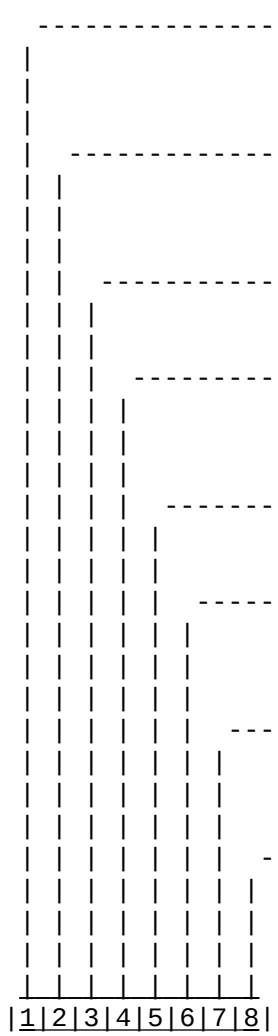
Bit(s)	Measurement	Contents
1	LLM-2A microprocessor lockout status	0=no MPLO 1=MPLO
2	LLM-2A self-test failure status	0=pass 1=fail
3	CC/DC in-process status	0=no cmd beginning execute 1=cmd beginning execute
4	LLM-2A POR status	0=no POR 1=one or more PORs, any power failure
5	LLM-2A microprocessor sync-idle error status	0=in sync 1=out of sync (1802 vs BIS) /idle lockup
6	CC/DC hardware buffer full status	0=empty 1=full
7	LLM-2A BA bus parity error status	0=no error 1=one or more errors, any BA involved
8	LLM-2A BA transaction parity error status	0=no error 1=one or more errors, LLM-2A BA involved

|1|2|3|4|5|6|7|8|

LLM2A ERROR WORD-1 IOSL-0 E-0473

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	LLM-2A TLM port memory read parity error status	0=no error 1=one or more parity errors when memory read by TLM port
2	LLM-2A microprocessor memory read parity error status	0=no error 1=one or more parity errors when memory read by processor
3	LLM-2A BA memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
4	engineering control port memory read parity error status	0=no error 1=one or more parity errors when memory read by engr. control port
5	CC/DC error status	0=overwrite not attempted 1=attempt to load CC/DC H/W buffer when already full
6	LLM-2A BA write protect error status	0=no error 1=write attempt by BA into protected memory, or I/O selects
7	LLM-2A microprocessor write protect error status	0=no error 1=write attempt by processor into protected memory
8	engineering data port write protect error status	0=no error 1=write attempt by engr. data port into protected memory



LLM2A ERROR WORD-2 IOSL-1 E-0474

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	LLM-2A MPLO	0=off	
		1=on	D
2	LLM-2A memory swap	0=off	
		1=on	D
3	LLM-2A CC/DC disable	0=off	
		1=on	D
4	LLM-2A bus select	0=BUS-2A	D
		1=BUS-2B	
5	LLM-2A bus adapter write protect	0=off	
		1=on	D
6	LLM-2A write protect 2000-2FFF/6000-6FFF	0=off	
		1=on	D
7	LLM-2A write protect 0000-1FFF/4000-5FFF	0=off	
		1=on	D
8	spare		

|1|2|3|4|5|6|7|8| HLM1B DESPUN CRC REGISTERS 0-3 (MSB) E-0653

Bit(s)	Measurement	Contents	
1	LLM-2B MPLO	0=off	
		1=on	D
2	LLM-2B Memory Swap	0=off	
		1=on	D
3	LLM-2B CC/DC disable	0=off	
		1=on	D
4	LLM-2B bus select	0=BUS-2A	D
		1=BUS-2B	
5	LLM-2B bus adapter write protect	0=off	
		1=on	D
6	LLM-2B write protect 2000-2FFF/6000-6FFF	0=off	
		1=on	D
7	LLM-2B write protect 0000-1FFF/4000-5FFF	0=off	
		1=on	D
8	spare		

|1|2|3|4|5|6|7|8| HLM1B DESPUN CRC REGISTERS 0-3 (2SB) E-0653

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	RRH-2 bus select	0=BUS-2A	D
		1=BUS-2B	
2	RRH-1 bus select	0=BUS-2A	
		1=BUS-2B	D
3	PPR bus select	0=BUS-2A	D
		1=BUS-2B	
4	NIMS bus select	0=BUS-2A	D
		1=BUS-2B	
5	SSI bus select	0=BUS-2A	D
		1=BUS-2B	
6	UVS bus select	0=BUS-2A	D
		1=BUS-2B	
7-8	spare		

HLM1B DESPUN CRC REGISTERS 0-3 (3SB) E-0653

Bit(s)	Measurement	Contents	
1	CRC-2B BA write busy error status	0=no error	
		1=write attempt when busy	
2	CRC-2B BA write protect error status	0=no error	
		1=error	
3	HCD transfer error status	0=no error	
		1=error	
4	HCD POR status	0=no POR	
		1=one or more PORs	
5	BUS-2B POR status	0=no POR	
		1=one or more PORs	
6	BUS-2A POR status	0=no POR	
		1=one or more PORs	
7	CRC-2B BA bus parity error status	0=no error	
		1=one or more errors, any BA involved	
8	CRC-2B BA transaction parity error status	0=no error	
		1=one or more errors, CRC-2B BA involved	

HLM1B DESPUN CRC REGISTERS 0-3 (LSB) E-0653 AND
HLM1B DESPUN CRC BANK B E-0655

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	spare		
2	backup MUX control BIT-C	0=reset 1=set	D
3	backup MUX control BIT-B	0=reset 1=set	D
4	backup MUX control BIT-A	0=reset 1=set	D
5	ADC-2A LLM select	0=LLM-2A 1=LLM-2B	D
6	IUS/STS-2B low rate TLM select	0=LLM-2A 1=LLM-2B	D
7	IUS/STS-2A low rate TLM select	0=LLM-2A 1=LLM-2B	D
8	CRC-2B critical enable master	0=off 1=on	

1|2|3|4|5|6|7|8| HLM1B DESPUN CRC REGISTERS 4-6 (MSB) E-0654

Bit(s)	Measurement	Contents	
1-4	spare		
5	CRC-2B bus adapter write protect	0=off 1=on	D
6	CRC-2B bus select	0=BUS-2A 1=BUS-2B	D
7	CRC-2A bus adapter write protect	0=off 1=on	D
8	CRC-2A bus select	0=BUS-2A 1=BUS-2B	D

1|2|3|4|5|6|7|8| HLM1B DESPUN CRC REGISTERS 4-6 (2SB) E-0654

Bit(s)	Measurement	Contents	
1-2	spare		
3	DESPUN critical enable 5 (spare)	0=reset 1=set	D
4	DESPUN critical enable 4 (spare)	0=reset 1=set	
5	DESPUN critical enable 3 (spare)	0=reset 1=set	
6	DESPUN critical enable 2 (probe umbilical cable cutter enable)	0=reset (ENABLE RESET) 1=set (ENABLE)	D
7	DESPUN critical enable 1 (PPS spare)	0=reset (ENABLE RESET) 1=set (ENABLE)	D
8	DESPUN critical enable 0 (probe release enable)	0=reset (ENABLE RESET) 1=set (ENABLE)	D

1|2|3|4|5|6|7|8| HLM1B DESPUN CRC REGISTERS 4-6 (LSB) E-0654

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

For the definition of E-0655, see HLM1B DESPUN CRC REGISTERS 0-3 (LSB) E-0653. Their definitions are identical.

HLM1B DESPUN CRC BANK B E-0655

Bit(s)	Measurement	Contents	
1	HLM-1A MPLO	0=off	
		1=on	D
2	HLM-1A memory swap	0=off	
		1=on	D
3	HLM-1A write protect	0=off	
	5000-5FFF/D000-DFFF	1=on	D
4	HLM-1A write protect	0=off	
	4000-4FFF/C000-CFFF	1=on	D
5	HLM-1A write protect	0=off	
	3000-3FFF/B000-BFFF	1=on	D
6	HLM-1A write protect	0=off	
	2000-2FFF/A000-AFFF	1=on	D
7	HLM-1A write protect	0=off	
	1000-1FFF/9000-9FFF	1=on	D
8	HLM-1A write protect	0=off	
	0000-0FFF/8000-8FFF	1=on	D

|1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK A REGISTERS 0-3 (MSB) E-0656

Bit(s)	Measurement	Contents	
1	LLM-1A MPLO	0=off	
		1=on	D
2	LLM-1A memory swap	0=off	
		1=on	D
3	LLM-1A CC/DC disable	0=off	
		1=on	D
4	LLM-1A bus select	0=BUS-1A	
		1=BUS-1B	D
5	LLM-1A bus adapter write protect	0=off	
		1=on	D
6	LLM-1A write protect	0=off	
	2000-2FFF/6000-6FFF	1=on	D
7	LLM-1A write protect	0=off	
	1000-1FFF/4000-5FFF	1=on	D
8	spare		

|1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK A REGISTERS 0-3 (2SB) E-0656

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	BUM-1A BA-2B write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
2	BUM-1A BA-2B write protect 1000-17FF/5000-57FF	0=off 1=on	D
3	BUM-1A BA-2B write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
4	BUM-1A BA-2B write protect 0000-07FF/4000-47FF	0=off 1=on	D
5	BUM-1A BA-1A write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
6	BUM-1A BA-1A write protect 1000-17FF/5000-57FF	0=off 1=on	D
7	BUM-1A BA-1A write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
8	BUM-1A BA-1A write protect 0000-07FF/4000-47FF	0=off 1=on	D

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK A REGISTERS 0-3 (3SB) E-0656

Bit(s)	Measurement	Contents	
1	BUM-1A TLM control BA select	0=BA-1A 1=BA-2B	D
2	Golay-1A bus select	0=BUS-1A 1=BUS-1B	D
3	BUM-1A BA-2B bus select	0=BUS-1A 1=BUS-1B	D
4	BUM-1A BA-1A bus select	0=BUS-1A 1=BUS-1B	D
5	BUM-1A memory swap	0=off 1=on	D
6	BUM-1A write protect 3000-37FF/7000-7FFF	0=off 1=on	D
7	BUM-1A write protect 2800-2FFF/6800-6FFF	0=off 1=on	D
8	BUM-1A write protect 2000-27FF/6000-67FF	0=off 1=on	D

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK A REGISTERS 0-3 (LSB) E-0656

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1-2	spare		
3	4.8 KHZ reference select	0=REF-1A	
		1=REF-1B	D
4-5	spare		
6	digital engineering serial-binary select	0=LLM-1A	
		1=LLM-1B	D
7	digital engineering timing chain select	0=TC-1A	
		1=TC-1B	D
8	CRC-1B critical enable master	0=off	
		1=on	

1|2|3|4|5|6|7|8 HLM1B SPUN CRC BANK A REGISTERS 4-6 (MSB) E-0657

1	HCD POR test control	0=off	
		1=on	D
2-4	spare		
5	HCD-1B override-3	0=on	
		1=off	
6	HCD-1B override-2	0=off	
		1=on	
7	HCD-1B override-1	0=off	
		1=on	
8	HCD-1A disable	0=off	
		1=on	

1|2|3|4|5|6|7|8 HLM1B SPUN CRC BANK A REGISTERS 4-6 (2SB) E-0657

1-2	spare		
3	spun critical enable 5 (spare)	0=reset	
		1=set	
4	spun critical enable 4 (RPN 2nd isolate and bypass enable)	0=reset (ENABLE RESET)	D
		1=set (ENABLE)	
5	spun critical enable 3 (AACS 400N engine enable)	0=reset (ENABLE)	
		1=set (DISABLE)	D
6	spun critical enable 2 (AACS memory B write protect)	0=reset	
		1=set	
7	spun critical enable 1 (AACS memory A write protect)	0=reset	
		1=set	*
8	spun critical enable 0 (spare)	0=reset	
		1=set	

1|2|3|4|5|6|7|8 HLM1B SPUN CRC BANK A REGISTERS 4-6 (LSB) E-0657

* Write protect disabled when opposing string is set similarly;
write protect enabled when opposing string is set differently.
D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

For the bit definition of E-0658, see HLM1B SPUN CRC STATUS WORD E-0668. Their definitions are identical.

HLM1B SPUN CRC BANK B E-0658

Bit(s)	Measurement	Contents	
1	HLM-1B MPLO	0=off	
		1=on	D
2	HLM-1B memory swap	0=off	
		1=on	D
3	HLM-1B write protect 5000-5FFF/D000-DFFF	0=off	
		1=on	D
4	HLM-1B write protect 4000-4FFF/C000-CFFF	0=off	
		1=on	D
5	HLM-1B write protect 3000-3FFF/B000-BFFF	0=off	
		1=on	D
6	HLM-1B write protect 2000-2FFF/A000-AFFF	0=off	
		1=on	D
7	HLM-1B write protect 1000-1FFF/9000-9FFF	0=off	
		1=on	D
8	HLM-1B write protect 0000-0FFF/8000-8FFF	0=off	
		1=on	D

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 0-3 (MSB) E-0659

1	LLM-1B MPLO	0=off	
		1=on	D
2	LLM-1B memory swap	0=off	
		1=on	D
3	LLM-1B CC/DC disable	0=off	
		1=on	D
4	LLM-1B bus select	0=BUS-1A	D
		1=BUS-1B	
5	LLM-1B bus adapter write protect	0=off	
		1=on	D
6	LLM-1B write protect 2000-2FFF/6000-6FFF	0=off	
		1=on	D
7	LLM-1B write protect 0000-1FFF/4000-5FFF	0=off	
		1=on	D
8	spare		

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 0-3 (2SB) E-0659

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	BUM-1B BA-2A write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
2	BUM-1B BA-2A write protect 1000-17FF/5000-57FF	0=off 1=on	D
3	BUM-1B BA-2A write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
4	BUM-1B BA-2A write protect 0000-07FF/4000-47FF	0=off 1=on	D
5	BUM-1B BA-1B write protect 1800-1FFF/5800-5FFF	0=off 1=on	D
6	BUM-1B BA-1B write protect 1000-17FF/5000-57FF	0=off 1=on	D
7	BUM-1B BA-1B write protect 0800-0FFF/4800-4FFF	0=off 1=on	D
8	BUM-1B BA-1B write protect 0000-07FF/4000-47FF	0=off 1=on	D
1|2|3|4|5|6|7|8	HLM1B SPUN CRC BANK B REGISTERS 0-3 (3SB) E-0659		
1	BUM-1B TLM control BA select	0=BA-1B 1=BA-2A	D
2	Golay-1B bus select	0=BUS-1A 1=BUS-1B	D
3	BUM-1B BA-2A bus select	0=BUS-1A 1=BUS-1B	D
4	BUM-1B BA-1B bus select	0=BUS-1A 1=BUS-1B	D
5	BUM-1B memory swap	0=off 1=on	D
6	BUM-1B write protect 3000-37FF/7000-7FFF	0=off 1=on	D
7	BUM-1B write protect 2800-2FFF/6800-6FFF	0=off 1=on	D
8	BUM-1B write protect 2000-27FF/6000-67FF	0=off 1=on	D
1|2|3|4|5|6|7|8	HLM1B SPUN CRC BANK B REGISTERS 0-3 (LSB) E-0659		

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	HIC/EUV bus select	0=BUS-1A	D
		1=BUS-1B	
2	DDS bus select	0=BUS-1A	D
		1=BUS-1B	
3	EPD bus select	0=BUS-1A	D
		1=BUS-1B	
4	PWS bus select	0=BUS-1A	D
		1=BUS-1B	
5	MAG bus select	0=BUS-1A	D
		1=BUS-1B	
6	PLS bus select	0=BUS-1A	D
		1=BUS-1B	
7	AACS-B bus select	0=BUS-1A	D
		1=BUS-1B	
8	AACS-A bus select	0=BUS-1A	
		1=BUS-1B	D

|1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 4-7 (MSB) E-0660

Bit(s)	Measurement	Contents	
1	DBUM-1B memory swap	0=OFF	
		1=ON	D
2	DBUM-1A memory swap	0=OFF	
		1=ON	D
3	spare		
4	HCD POR test select	0=PC-1A	
		1=PC-1B	D
5	timing chain manual	0=off	
	select control	1=on	D
6	timing chain manual	0=TC-1A	
	select	1=TC-1B	D
7	POR fault override	0=off	
	control	1=on	D
8	POR fault override	0=PC-1A	
	select	1=PC-1B	D

|1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 4-7 (2SB) E-0660

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents	
1	spare		
2-3	hi rate TLM mod TMU-1B select	00=LLM-1A (Note 1) 01=BUM-1A 10=LLM-1B 11=BUM-1B	
4	low rate TLM mod TMU-1B select	0=LLM-1A 1=LLM-1B	D
5	spare		
6-7	hi rate TLM mod TMU-1A select	00=LLM-1A (Note 2) 01=BUM-1A 10=LLM-1B 11=BUM-1B	
8	low rate TLM mod TMU-1A select	0=LLM-1A 1=LLM-1B	D

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 4-7 (3SB) E-0660

1	spare DBUM select	0=DBUM-1A 1=DBUM-1B	D
2	DBUM-1B bus select	0=BUS-1A 1=BUS-1B	D
3	DMS DBUM select	0=DBUM-1A 1=DBUM-1B	D
4	DBUM-1A bus select	0=BUS-1A 1=BUS-1B	D
5	CRC-1B bus adapter write protect	0=off 1=on	D
6	CRC-1B bus select	0=BUS-1A 1=BUS-1B	D
7	CRC-1A bus adapter write protect	0=off 1=on	D
8	CRC-1A bus select	0=BUS-1A 1=BUS-1B	D

1|2|3|4|5|6|7|8| HLM1B SPUN CRC BANK B REGISTERS 4-7 (LSB) E-0660

D=Dependent. This state only occurs when the opposing string's CRC bit is set similarly

Note 1 - The LLM's are the source only if both strings' CRC bit 3 are reset (logical 0).
The A string (LLM or BUM is the source only if both strings' CRC bit 2 are reset (logical 0).

Note 2 - The LLM's are the source only if both strings' CRC bit 7 are reset (logical 0).
The B string (LLM or BUM) is the source only if both strings' CRC bit 6 are set (logical 1).

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-6	HCD-1B command message number	6 LSBs of cmd message sent to HCD-1B
7	HCD-1B message start word bit error status	0=error-free start word 1=error in start word
8	HCD-1B uplink message disposition	0=accepted 1=rejected

|1|2|3|4|5|6|7|8| HLM1B HCD COMMAND SUMMARY WORD E-0661

1-8	HCD-1B messages received and accepted counter	increments by one for each message accepted by HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B MSG RCVD AND ACCEPTED COUNTER E-0662

1-8	HCD-1B messages received and rejected counter	increments by one for each message rejected by HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B MSG RCVD AND RJCTD COUNTER E-0663

1-8	HCD-1B command frame errors detected counter	increments by one for each command frame detected with errors by HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B CMD FRAME ERRORS DETECTED COUNTER E-0664

1-8	HCD-1B data frame errors corrected counter	increments by one for each data frame corrected by HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B DATA FRAME ERRORS CORRECTED COUNTER E-0665

1-8	HCD-1B data frame errors uncorrectable counter	increments by one for each erroneous data frame uncorrectable by HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B DATA FRAME ERRORS UNCORRECTABLE COUNTER E-0666

1-8	HCD-1B lock changes counter	increments by one for each lock change provided to HCD-1B (MOD 256)

|1|2|3|4|5|6|7|8| HLM1B LOCK CHANGES COUNTER E-0667

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	CRC-1B BA write busy error status	0=no error 1=write attempt when busy
2	CRC-1B BA write protect error status	no error 1=error
3	CRC-1B command block write attempt	0=no attempt 1=one or more attempts
4	CRC-1B power converter/ HCD POR status	0=no POR 1=one or more PORs
5	spare	
6	multiple frame CMD with zero data frames	0=no error 1=one or more errors
7	CRC-1B BA BUS parity error status	0=no error 1=one or more errors, any BA involved
8	CRC-1B BA transaction parity error status	0=no error 1=one or more errors, CRC-1B BA involved

|1|2|3|4|5|6|7|8|

HLM1B SPUN CRC STATUS WORD E-0668 AND
HLM1B SPUN CRC BANK A E-0658

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	BUS-1B overrun status	0=no overrun 1=overrun error, bus trans-action in process at RTI
2	HLM-1B self-test failure status	0=pass 1=fail
3	HLM-1B keep-alive POR status	0=no KAPOR 1=one or more KAPORs with memory loss
4	HLM-1B POR status	0=no POR 1=one or more PORs, any power failure
5	HLM-1B microprocessor sync-idle error status	0=in sync 1=out of sync (1802 vs BIS) /idle lockup
6	HLM-1B BA bus parity error status - despun mux	0=no error 1=one or more errors, any BA involved (DESPUN MUX)
7	HLM-1B BA bus parity error status	0=no error 1=one or more errors, any BA involved(BC or SPUN MUX)
8	HLM-1B BA transaction parity error status	0=no error 1=one or more errors, HLM-1B BA involved

|1|2|3|4|5|6|7|8|

HLM1B ERROR WORDS IOSL 0-1-2 (MSB) E-0669

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	HCD parity error status	0=no error 1=one or more parity errors from HCD to HLM-1B
2	HLM-1B microprocessor memory read parity error status	0=no error 1=one or more parity errors when memory read by processor
3	HLM-1B BA memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
4	HLM-1B bus controller memory read parity error status	0=no error 1=one or more parity errors when memory read by BC
5	HLM-1B microprocessor lockout status	0=no MPLO 1=MPLO
6	HLM-1B BA write protect error status	0=no error 1=write attempt by BA into protected memory
7	HLM-1B microprocessor write protect error status	0=no error 1=write attempt by processor into protected memory
8	HCD write protect error status	0=no error 1=write attempt by HCD into protected memory

|1|2|3|4|5|6|7|8| HLM1B ERROR WORDS IOSL 0-1-2 (2SB) E-0669

Bit(s)	Measurement	Contents
1-2	grounded spare	0
3	PLL-1B timing chain select status	0=timing chain A 1=timing chain B
4	PLL-1A timing chain select status	0=timing chain A 1=timing chain B
5-6	grounded spare	0
7	phase locked loop 1B POR status	0=no POR 1=one or more PORs
8	phase locked loop 1A POR status	0=no POR 1=one or more PORs

|1|2|3|4|5|6|7|8| HLM1B ERROR WORDS IOSL 0-1-2 (LSB) E-0669

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-3	spare	
4	BUM-1A POR status	0=no POR 1=one or more PORs
5	BUM-1A BA-2B bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
6	BUM-1A BA-2B transaction parity error status	0=no error 1=one or more parity errors involving BUM-1A's BA-2B
7	BUM-1A BA-1A bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
8	BUM-1A BA-1A transaction parity error status	0=no error 1=one or more parity errors involving BUM-1A's BA-1A

|1|2|3|4|5|6|7|8| HLM1B BUM ERROR WORDS (MSB) E-0671

1	BUM-1A telemetry formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
2	BUM-1A telemetry sequencer memory read parity error status	0=no error 1=one or more parity errors when memory read by sequencer
3	BUM-1A BA-2B memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-2B
4	BUM-1A BA-1A memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-1A
5-6	spare	
7	BUM-1A BA-1A write protect error status	0=no error 1=write attempt by BA-2B into protected memory
8	BUM-1A BA-1A write protect error status	0=no error 1=write attempt by BA-1A into protected memory

|1|2|3|4|5|6|7|8| HLM1B BUM ERROR WORDS (2SB) E-0671

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1-3	spare	
4	BUM-1B POR status	0=no POR 1=one or more PORs
5	BUM-1B BA-2A bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
6	BUM-1B BA-2A transaction parity error status	0=no error 1=one or more parity errors involving BUM-1B's BA-2A
7	BUM-1B BA-1B bus parity error status	0=no error 1=one or more parity errors involving any BA on its bus
8	BUM-1B BA-1B transaction parity error status	0=no error 1=one or more parity errors involving BUM-1B's BA-1B

|1|2|3|4|5|6|7|8| HLM1B BUM ERROR WORDS (3SB) E-0671

1	BUM-1B telemetry formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
2	BUM-1B telemetry sequencer memory read parity error status	0=no error 1=one or more parity errors when memory read by sequencer
3	BUM-1B BA-2A memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-2A
4	BUM-1B BA-1B memory read parity error status	0=no error 1=one or more parity errors when memory read by BA-1B
5-6	spare	
7	BUM-1B BA-2A write protect error status	0=no error 1=write attempt by BA-2A into protected memory
8	BUM-1B BA-1B write protect error status	0=no error 1=write attempt by BA-1B into protected memory

|1|2|3|4|5|6|7|8| HLM1B BUM ERROR WORDS (LSB) E-0671

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	DMS illegal command status	0=no illegal command 1=illegal cmd (not per DMS CMD dictionary)
2	DBUM-1A sequencer output memory read parity error status	0=no error 1=one or more parity errors when memory read by DBUM sequencer
3	DBUM-1A formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
4	DBUM-1A bus adapter memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
5	DMS tape direction status	0=forward 1=reverse
6	DBUM-1A POR status	0=no POR 1=one or more PORs
7	DBUM-1A bus adapter bus parity error status	0=no error 1=one or more parity errors involving any BA
8	DBUM-1A BA transaction parity error status	0=no error 1=one or more parity errors involving DBUM-1A BA

|1|2|3|4|5|6|7|8| HLM1B DBUM ERROR WORDS (MSB) E-0672 Note 1

Note 1 - This data not valid unless DBUM-1A switched to B string.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	DMS illegal command status	0=no illegal command 1=illegal cmd (not per DMS CMD dictionary)
2	DBUM-1B sequencer output memory read parity error status	0=no error 1=one or more parity errors when memory read by DBUM sequencer
3	DBUM-1B formatter memory read parity error status	0=no error 1=one or more parity errors when memory read by formatter
4	DBUM-1B bus adapter memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
5	DMS tape direction status	0=forward 1=reverse
6	DBUM-1B POR status	0=no POR 1=one or more PORs
7	DBUM-1B bus adapter bus parity error status	0=no error 1=one or more parity errors involving any BA
8	DBUM-1B BA transaction parity error status	0=no error 1=one or more parity errors involving DBUM-1B BA

|1|2|3|4|5|6|7|8| HLM1B DBUM ERROR WORDS (LSB) E-0672 Note 1

Bit(s)	Measurement	Contents
1	LLM-1B microprocessor lockout status	0=no MPLO 1=MPLO
2	LLM-1B self-test failure status	0=pass 1=fail
3	CC/DC in-process status	0=no cmd beginning execute 1=cmd beginning execute
4	LLM-1B POR status	0=no POR 1=one or more PORs, any power failure
5	LLM-1B microprocessor sync-idle error status	0=in sync 1=out of sync (1802 vs BIS) /idle lockup
6	CC/DC hardware buffer full status	0=empty 1=full
7	LLM-1B BA bus parity error status	0=no error 1=one or more errors, any BA involved
8	LLM-1B BA transaction parity error status	0=no error 1=one or more errors, LLM-1B BA involved

|1|2|3|4|5|6|7|8| LLM1B ERROR WORD-1 IOSL-0 E-0913

Note 1 - This data not valid unless DBUM-1B switched to B string.

Table A2.2.9 Digital and Software Bit Definitions (Bit 1 is MSB)

Bit(s)	Measurement	Contents
1	LLM-1B TLM port memory read parity error status	0=no error 1=one or more parity errors when memory read by TLM port
2	LLM-1B microprocessor memory read parity error status	0=no error 1=one or more parity errors when memory read by processor
3	LLM-1B BA memory read parity error status	0=no error 1=one or more parity errors when memory read by BA
4	engineering control port memory read parity error status	0=no error 1=one or more parity errors when memory read by engr. control port
5	CC/DC error status	0=overwrite not attempted 1=attempt to load CC/DC H/W buffer when already full
6	LLM-1B BA write protect error status	0=no error 1=write attempt by BA into protected memory, or I/O selects
7	LLM-1B microprocessor write protect error status	0=no error 1=write attempt by processor into protected memory
8	engineering data port write protect error status	0=no error 1=write attempt by engr. data port into protected memory

|1|2|3|4|5|6|7|8| LLM1B ERROR WORD-2 IOSL-1 E-0914

1	DMS BOT/EOT status	0=BOT 1=EOT
2	DMS leader/tape status	0=on tape 1=on leader
3-8	tic count status (6 MSB)	6 MSBs of the 14 bit tic count

|1|2|3|4|5|6|7|8| LLM1B DMS TAPE POSITION ESTIMATE MSB E-0923

1-8	tic count status (8 LSB)	8 LSBs of the 14 bit tic count

|1|2|3|4|5|6|7|8| LLM1B DMS TAPE POSITION ESTIMATE LSB E-0924

A2.2.14.4 CDS Treeswitch Assignments. Table A2.2.10 identifies the usage of CDS treeswitch positions by reference to the engineering measurementnumbers defined in Table A2.2.8.

Table A2.2.10 CDS Treeswitch Assignments

Tree Position	Tree T1A	T1B	T2A	T2B
00	E-0018	E-0019	E-1665	E-1666
01	E-0065	E-0066	E-0067	E-0068
02	E-1635	E-1636	E-1950	E-1951
03	E-0058	E-0062	not avail.	not avail.
04	E-0057 (MSB)	E-0061 (MSB)	not avail.	not avail.
05	E-0057 (LSB)	E-0061 (LSB)	not avail.	not avail.
06	not avail.	not avail.	not avail.	not avail.
07	not avail.	not avail.	not avail.	not avail.
08	E-0020	E-0052	not avail.	not avail.
09	E-0053	E-0021	not avail.	not avail.
0A	E-0055	E-0059	not avail.	not avail.
0B	E-0056	E-0060	not avail.	not avail.
0C	E-1650	E-1651	not avail.	not avail.
0D	not avail.	not avail.	not avail.	not avail.
0E	not avail.	not avail.	not avail.	not avail.
0F	not avail.	not avail.	not avail.	not avail.
10	E-1100	E-1120	spare	not avail.
11	E-1101	E-1121	spare	not avail.
12	E-1102	E-1122	spare	not avail.
13	E-1103	E-1123	spare	not avail.
14	E-1104	E-1124	spare	not avail.
15	E-1105	E-1125	E-0071	not avail.
16	E-1106	E-1126	spare	not avail.
17	E-1107	E-1127	spare	not avail.
18	E-0080	E-0081	E-0092	not avail.
19	E-0042	E-0101	spare	not avail.
1A	E-1585	E-0102	spare	not avail.
1B	E-0030	E-0040	spare	not avail.
1C	E-0039	E-0103	spare	not avail.
1D	E-0078	E-0104	spare	not avail.
1E	E-0105	E-1506	spare	not avail.
1F	E-1141	E-1148	E-1155	not avail.
20	E-1586	E-1589	spare	not avail.
21	E-0107	E-0041	spare	not avail.
22	E-0108	E-0106	spare	not avail.
23	E-0082	E-0083	spare	not avail.
24	E-0031	E-0027	spare	not avail.
25	spare	spare	E-1136	not avail.
26	E-0109	E-1500	E-0077	not avail.
27	E-1501	E-0070	E-0093	not avail.
28	E-1108	E-1128	spare	not avail.
29	E-1505	E-1507	spare	not avail.

Table A2.2.10 CDS Treeswitch Assignments (Cont'd)

Tree Position	Tree T1A	T1B	T2A	T2B
2A	E-0032	E-0037	spare	not avail.
2B	E-0095	E-0094	E-0072	not avail.
2C	E-1680	E-1590	spare	not avail.
2D	E-0034	E-0029	spare	not avail.
2E	E-1110	E-1130	spare	not avail.
2F	E-1142	E-1149	E-1156	not avail.
30	E-1652	E-1653	spare	not avail.
31	spare	E-1553	E-1970	not avail.
32	E-1980	E-1981	spare	not avail.
33	E-0024	E-0022	spare	not avail.
34	spare	E-0088	spare	not avail.
35	spare	spare	spare	not avail.
36	E-1551	E-0016	spare	not avail.
37	E-1552	spare	E-0079	not avail.
38	E-0038	E-0025	spare	not avail.
39	E-1591	E-1587	spare	not avail.
3A	spare	spare	spare	not avail.
3B	spare	E-0033	spare	not avail.
3C	E-0073	spare	E-0074	not avail.
3D	spare	E-1720	spare	not avail.
3E	E-0086	spare	spare	not avail.
3F	E-1143	E-1150	E-1157	not avail.
40	E-0090	E-0091	spare	not avail.
41	spare	E-0036	spare	not avail.
42	spare	E-1556	spare	not avail.
43	spare	E-0087	spare	not avail.
44	E-1588	spare	spare	not avail.
45	spare	spare	spare	not avail.
46	E-0023	E-0026	spare	not avail.
47	spare	spare	spare	not avail.
48	spare	spare	spare	not avail.
49	spare	E-1594	spare	not avail.
4A	E-0069	E-0075	spare	not avail.
4B	E-1109	E-1129	E-1960	not avail.
4C	E-0028	E-0035	spare	not avail.
4D	spare	spare	E-0076	not avail.
4E	E-1486	E-1487	spare	not avail.
4F	E-1144	E-1151	E-1158	not avail.
50	E-1660	E-1659	E-1952	not avail.
51	E-1613	E-1595	E-1910	not avail.
52	E-1643	E-1608	E-1913	not avail.
53	E-1607	E-1649	E-0009	not avail.
54	E-0097	E-1640	E-1915	not avail.

Table A2.2.10 CDS Treeswitch Assignments (Cont'd)

Tree Position	Tree T1A	T1B	T2A	T2B
55	E-1860	E-1604	E-1883	not avail.
56	E-1648	E-1485	E-1473	not avail.
57	E-0043	E-1863	E-1967	not avail.
58	E-1639	E-1644	E-1479	not avail.
59	E-1690	E-0100	E-1715	not avail.
5A	E-1618	E-1948	E-1475	not avail.
5B	E-0045	E-0050	E-0011	not avail.
5C	E-1600	E-1693	E-0008	not avail.
5D	E-1740	E-1751	E-1885	not avail.
5E	E-0000	E-0001	E-1916	not avail.
5F	E-1145	E-1152	E-1159	not avail.
60	E-1657	E-1612	E-1625	not avail.
61	E-0044	E-0046	E-1953	not avail.
62	E-1615	E-1722	E-1912	not avail.
63	E-1610	E-1609	E-1914	not avail.
64	E-1606	E-1605	E-1790	not avail.
65	E-1645	E-1641	E-1480	not avail.
66	E-1619	E-0003	E-0012	not avail.
67	E-0048	E-0051	E-0014	not avail.
68	E-1478	E-1477	E-1880	not avail.
69	E-1638	E-1692	E-1647	not avail.
6A	E-0004	E-1617	E-1966	not avail.
6B	E-1862	E-1982	E-1474	not avail.
6C	E-1602	E-1753	E-1481	not avail.
6D	E-1750	E-0098	E-1884	not avail.
6E	E-1557	E-0049	E-0015	not avail.
6F	E-1146	E-1153	E-1160	not avail.
70	E-1642	E-1658	E-1911	not avail.
71	E-1596	E-1620	E-1882	not avail.
72	E-1681	E-1614	E-1954	not avail.
73	E-1611	E-0017	spare	not avail.
74	E-1603	E-1599	E-1881	not avail.
75	E-1675	E-1646	E-1482	not avail.
76	E-0002	E-1472	E-1965	not avail.
77	E-0047	E-0005	E-0010	not avail.
78	E-1598	E-1597	E-1946	not avail.
79	E-1691	E-1861	E-1716	not avail.
7A	E-1483	E-1676	E-1476	not avail.
7B	E-0096	E-1616	E-0013	not avail.
7C	E-1752	E-1601	E-1947	not avail.
7D	E-0099	E-1637	E-1945	not avail.
7E	E-0006	E-0007	E-1968	not avail.
7F	E-1147	E-1154	E-1161	not avail.

A2.3 Memory Readout Data

A2.3.1 Memory Readout Structure. The spacecraft data system shall provide a common structure for reading out any onboard computer memory. The structure shall support both 8 and 16 bit memory readouts.

The format of this structure is shown in Figure A2.3.1 and described in greater detail in Table A2.3.1.

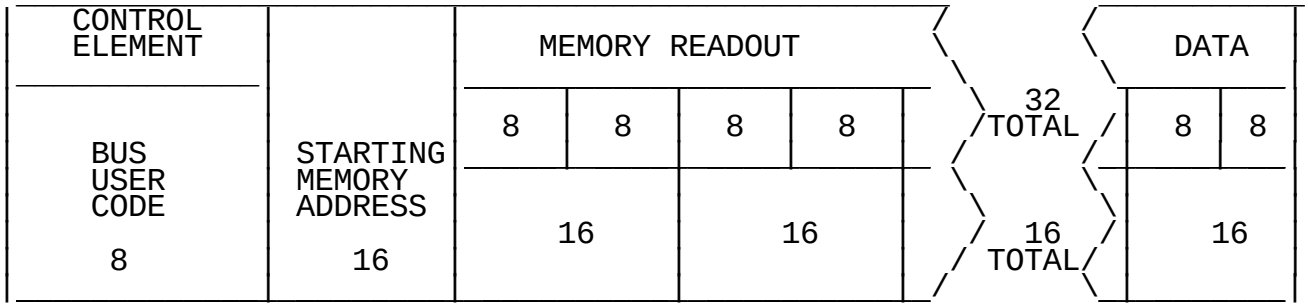


Figure A2.3.1. Memory Readout Structure

Table A2.3.1. Memory Readout Structure

Data Description	Bits/frame	Offset to Data Start	Paragraph
Bus User Code	8	0	A2.3.1.1
Starting Address	16	8	A2.3.1.2
Memory Readout Data	256	24	A2.3.1.3

A2.3.1.1 Bus User Codes. The Bus User Code area contains Bus source codes, and describes the data contained within the memory readout portion of the frame. The contents shall be interpreted in accordance with Table A2.3.2.

Table A2.3.2. Bus User Codes

Subsystem/ Module	Bus User (source) code	Data Field Width (bits)	Number of words in Frame
EPD	99	8	32
PPR	9B	8	32
*EUV/HIC	9C	8	32
DDS	9D	8	32
PLS	A0	8	32
UVS	A2	8	32
MAG	A3	8	32
SSI	A4	8	32
NIMS	A5	8	32
AACS-A	87	16	16
AACS-B	88	16	16
RRH-1	B4	8	32
RRH-2	B7	8	32
CDS			
HLM-1A	84	8	32
HLM-1B	85	8	32
LLM-1A	8C	8	32
LLM-1B	8D	8	32
LLM-2A	AC	8	32
LLM-2B	AD	8	32
BUM-1A-1A	90	8	32
BUM-1A-2B	91	8	32
BUM-1B-1B	94	8	32
BUM-1B-2A	95	8	32
DBUM-1A	8A	8	32
DBUM-1B	8B	8	32
CRC-1A	8E	8	32
CRC-1B	8F	8	32
CRC-2A	AE	8	32
CRC-2B	AF	8	32

* HIC has no MRO capability; EUV does

A2.3.1.2 Starting Address. This field shall represent the address corresponding to the first memory readout word in the readout data.

In order to provide a consistent readout format for all spacecraft computer memories, the memory readout shall start at a specified address.

A2.3.1.3 Memory Readout Data. The data in this portion of the frame shall contain the contents of consecutive memory locations. The first data word shall be the contents of the memory location specified by the starting address field.

A2.3.1.3.1 Subsystem Memory. For any subsystem commanded memory readout, the number of consecutive memory locations read out per block shall be 16 or 32 corresponding to 16 or 8 bit processor word sizes respectively.

A2.3.1.3.2 Commutation Map Readout Data. In order to facilitate ground reconstruction of on-board engineering commutation maps, the maps shall be stored in a known location. In the event that the Orbiter partitions the engineering commutation maps among various CDS and AACS memories, the various partitions shall all be stored in known locations.

A2.3.2 Data Frame Replacement Readout. The spacecraft data system shall have the capability to read out any on-board processor memory in the engineering data stream. The format of the data frame replace-ment memory readout shall be as shown in Figure A2.3.2.

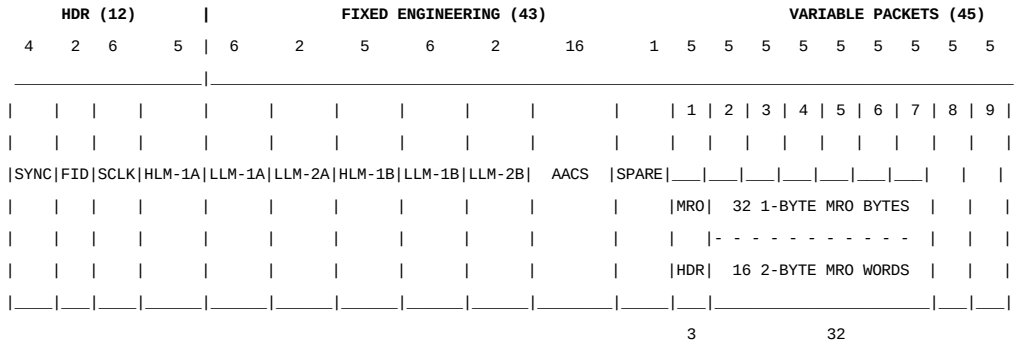


Figure A 2.3.2. Data Frame Replacement Memory Readout

A2.3.2.1 Description. The CDS shall collect the memory readout data from the desired subsystem and create a memory readout structure identical to paragraph A2.3.1. This structure will replace the last 56th through 91st bytes in the engineering frame.

A2.3.3 Memory Readout Data Stream. The Sequence in which the 32-byte blocks of memory readout data appear in the engineering telemetry is dependent on both the engineering telemetry data rate and the memory readout mode selected within the CDS, as described in the following paragraphs.

A2.3.3.1 Memory Readout within 1200 b/s Engineering. Successive frames of the high rate engineering (EHR) shall contain 32-byte blocks of memory readout data from sequential locations when the high rate (EHR) memory readout mode is selected.

A2.3.3.2 Memory Readout within 40 b/s Engineering. Successive frames of 40 b/s snapshot engineering (ESS) shall contain 32-byte blocks of memory readout data from sequential locations when the snapshot memory readout mode is selected. During the time of read-out, the CDS-internal EHR buffers will contain an unchanging MRO block for 30 of its 1200 bps frames.

A2.3.3.2A Memory Readout Within 16 b/s Engineering.

DELETED FOR PHASE 2

A2.3.3.2B Memory Readout Within 10 b/s Engineering. Successive frames of 10 b/s snapshot engineering (ELS) shall contain 32 byte blocks of memory readout data from sequential locations when the low ratre memory readout mode is selected. During the time of read-out, the CDS-internal EHR buffers will contain an unchanging MRO block for 120 of its 1200 bps frames.

A2.3.3.2C Memory Readout Within 8 b/s Engineering.

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A2.3.3.2D Memory Readout Within 2 b/s Engineering. Successive frames of 2 b/s snapshot engineering (EXS) shall contain 32 byte blocks of memory readout data from sequential locations when the very low rate memory readout mode is selected. During the time of read-out, the CDS-internal EHR buffers will contain an unchanging MRO block for 600 of its 1200 bps frames.

A2.3.4 Memory Readout Sampling Time. All memory readout data shall be sampled between 476-2/3 and 533-1/3 milliseconds after the SCLK contained in the engineering frame header containing the readout.

A2.4 AACS POSITION AND RATE DATA

The AACS shall provide pointing vector and rate data. The pointing vector information shall be provided in the Earth Mean Equator (EME) 1950.0 coordinate system, the Ecliptic (ECL) 1950.0 coordinate system, and spacecraft relative coordinate system. The data packet schematic is shown in Figure A2.4.1 and described further in Table A2.4.1.

The AACS P&R data is encoded into 3 separately sized data packages for inclusion in four TDM Telemetry Formats. These inclusions are as indicated in Figure A2.4.1 and are described below.

- LPW & LNR: the full 12 word (192 bits) packet
- LPU : the first 6 words (96 bits) of the packet
- BPT : the 4th & 5th words (32 bits) of the packet

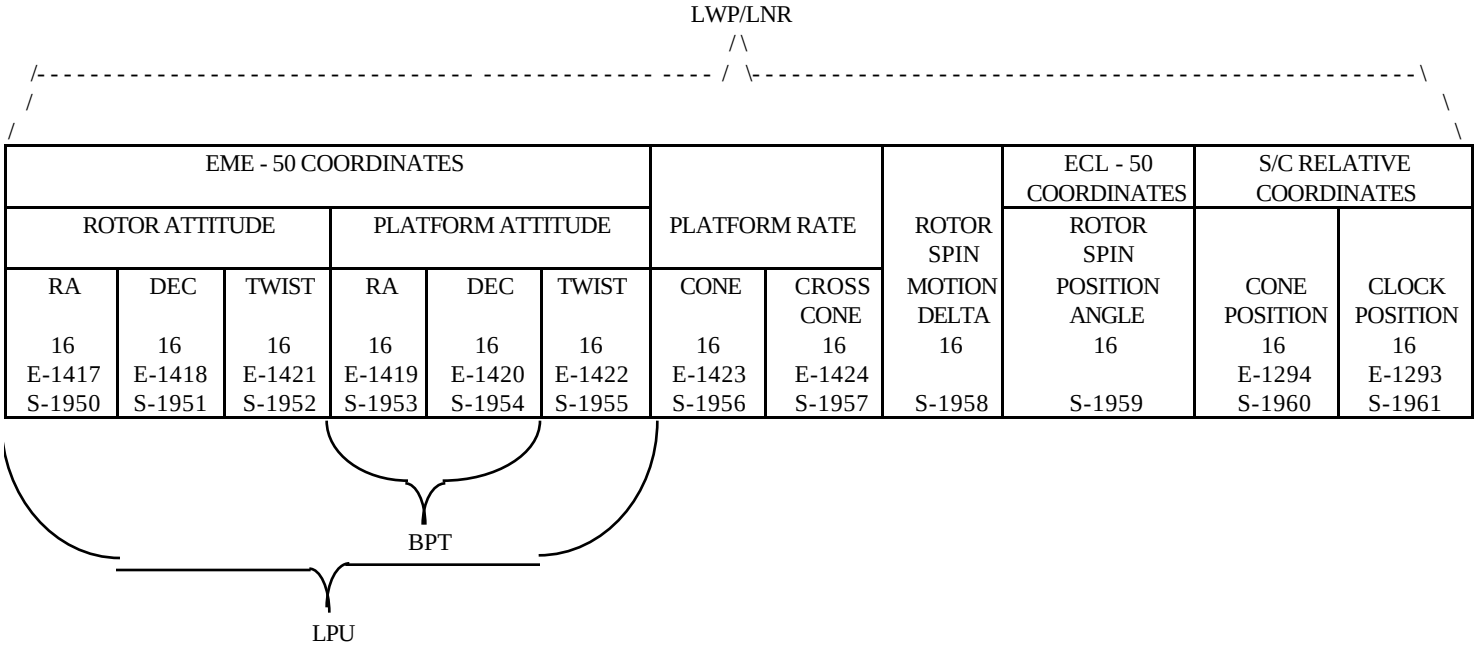


Figure A2.4.1. AACS Position and Rate Data

Table A2.4.1. AACS Position and Rate Data

Data Description	Bits Frame	Data Start	Comments(1)
Rotor Attitude (2)			The Least Significant Bit (LSB)
Right Ascension (RA)	16	0	represents $1/2^{16}$ revolution.
Declination (DEC)	16	16	
Twist (3)	16	32	
Platform Attitude (2)			The Least Significant Bit (LSB)
Right Ascension (RA)	16	48	represents $1/2^{16}$ revolution.
Declination (DEC)	16	64	
Twist (4)	16	80	
Platform Rate			The LSB represents $1/2^{16}$ revolution
Cone	16	96	during 8-1/3 millisecond interval.
Cross Cone	16	112	
Rotor Spin Motion Delta	16	128	The LSB represents $1/2^{16}$ revolution during 8-1/3 millisecond interval.
Rotor Spin Position Angle (2,5)	16	144	The LSB represents $1/2^{16}$ revolution
Cone Position (2,6)	16	160	The LSB represents $1/2^{16}$ revolution
Clock Position (2,7)	16	176	

Notes:

(1) Data is a 16 bit 2's complement number.

(2) Data is predicted ahead to RTI 0.

(3) Rotor twist represents rotation about the spacecraft Z-axis. The twist angle shall be defined as the angle from the projection of the Earth's North Pole onto the X-Y plane to the Rotor -X-axis (positive rotation about the Z-axis provides a positive twist angle.)

(4) Platform twist represents rotation about the scan platform boresight (L-axis). The twist angle shall be defined as the angle from the projection of the Earth's North Pole onto the M-N plane to the scan platform -M-axis (positive rotation about the L-axis provides a positive twist angle.

(5) Spin position angle represents the angle from the projection of the North Ecliptic Pole vector on the X-Y plane to the -X-axis. Positive rotation about the Z-axis provides a positive spin position angle.

(6) Cone position represents the null offset corrected encoder angle between the -Z-axis and the scan platform boresight (L-axis). An increasing encoder reading represents an increasing +N rotation of the scan platform with respect to the stator.

(7) Clock position represents the null offset corrected angle between the -Y-axis of the rotor and the SAS shaft (-N-axis, nominally the -Y-axis of the stator). An increasing encoder reading represents an increasing -Z rotation of the rotor with respect to the stator.

A2.5 DUST DETECTOR SUBSYSTEM TELEMETRY

This paragraph describes the format and content of the DDS output.

A2.5.1 DDS Packet. The schematic of this packet is shown in Figure A2.5.1. One full DDS packet is distributed over 13 LPW/LNR frames.

Title	DDS Science Data	Digital Status and Analog Engineering
Data Offset	0	120
Bits/packet	120	88
Description	A2.5.3	A2.5.4

Figure A2.5.1 DDS Packet

A2.5.2 Instrument Synchronicity. Within the DDS packet, there will exist one major synchronism relative to the SCLK. The relationship of the start of the DDS packet to SCLK and synchronization index (SI) is shown in Table A2.5.1.

Table A2.5.1 Relationship of SI and SCLK to start of DDS packet

SI	MOD 91	DDS Packet #
0	1	1st packet
1	14	2nd packet
2	27	3rd packet
3	40	4th packet
4	53	5th packet
5	66	6th packet
6	79	7th packet

A2.5.3 DDS Science Data. The DDS Science Data section may contain 3 different data types, dependant on the mode selected. Mode 1 is the science collection mode. The first 15 bytes of data (1 through 15) contain dust detection information. The contents of this section are then shown in Table A2.5.2.

Mode 2 is a memory read-out mode. In the memory readout mode, the first byte of DDS data contains the 8 MSB's of the starting address of the memory readout, and the next byte contains the 8 LSB's of the starting address. The next 13 bytes of data (3 through 15) contain memory readout data.

Table A2.5.2 DDS Science Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-6	ion grid amplifier output	10^{-14} to 10^{-8} Coulombs
7-8	ion grid threshold	threshold value in binary

|1|2|3|4|5|6|7|8| DDS Byte 1

1	threshold status	0=commanded 1=automatic
2-6	channeltron output	10^{-12} to 10^{-10} Coulombs
7-8	channeltron threshold	threshold value in binary

|1|2|3|4|5|6|7|8| DDS Byte 2

1-6	target pulse amplifier output	10^{-14} to 10^{-8} Coulombs
7-8	electron pulse threshold	threshold value in binary

|1|2|3|4|5|6|7|8| DDS Byte 3

1-6	entrance grid amplitude output	10^{-15} to 10^{-11} Cb(neg.) 10^{-15} to 10^{-13} Cb(pos.)
7-8	primary pulse threshold	threshold value in binary

|1|2|3|4|5|6|7|8| DDS Byte 4

1-5	entrance grid-target flighttime	1 to 400 microseconds
6-8	event definition	000=any channel 001=Qc, Qi 010=Qc, Qe 011=Qc 100=Qi, Qe 101=Qi 110=Qe 111=n/a

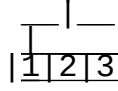
|1|2|3|4|5|6|7|8| DDS Byte 5

1-4	target pulse risetime	10 to 100 microseconds
5-8	ion grid pulse risetime	10 to 100 microseconds

|1|2|3|4|5|6|7|8| DDS Byte 6

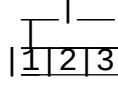
Table A2.5.2 DDS Science Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-4	target-ion grid flighttime	1 to 50 microseconds
5	target-ion grid coincidence	0=no coincidence 1=coincidence
6	ion grid-channeltron coincidence	0=no coincidence 1=coincidence
7-8	event class number	class number in binary



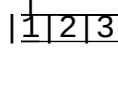
DDS Byte 7

1-4	measurement of entrance grid noise pulses detected	binary number
5-8	target noise pulses detected	binary number



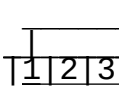
DDS Byte 8

1-4	ion grid noise pulses detected	binary number
5-8	channeltron noise pulses detected	binary number



DDS Byte 9

1-8	class counter 0	binary count



DDS Byte 10

1-8	class counter 1	binary count

DDS Byte 11

1-8	class counter 2	binary count

DDS Byte 12

1-8	class counter 3	binary count

DDS Byte 13

Table A2.5.2 DDS Science Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-4	S/C time of event	4 LSB of RIM
5-8	S/C time of event	bits 2 through 5 of MOD 91 count

|1|2|3|4|5|6|7|8| DDS Byte 14

Bit(s)	Measurement	Contents
1-8	sector data	8 MSB of sum of spin position angle and spin motion delta

|1|2|3|4|5|6|7|8| DDS Byte 15

Mode 3 is the instrument set point. In the set point mode, two packets of DDS data will contain set point data. The first packet of data is identified by byte 16 as being set points 1. This packet will contain 15 bytes of set point data, as identified in Table A2.5.3. The next DDS packet will be identified by byte 16 as being set points 2, and will contain 5 bytes of set point data and 10 bytes of random fill data.

Table A2.5.3 DDS Instrument Set Point Data

Bit(s)	Measurement	Contents
1-8	IT threshold, low level	0 to 255, commandable

|1|2|3|4|5|6|7|8| DDS set points 1 Byte 1

Bit(s)	Measurement	Contents
1-8	IT threshold, high level	0 to 255, commandable

|1|2|3|4|5|6|7|8| DDS set points 1 Byte 2

Bit(s)	Measurement	Contents
1-8	ET threshold, low level	0 to 255, commandable

|1|2|3|4|5|6|7|8| DDS set points 1 Byte 3

Bit(s)	Measurement	Contents
1-8	ET threshold, high level	0 to 255, commandable

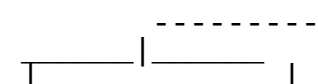
|1|2|3|4|5|6|7|8| DDS set points 1 Byte 4

Bit(s)	Measurement	Contents
1-8	EIT threshold, low level	0 to 255, commandable

|1|2|3|4|5|6|7|8| DDS set points 1 Byte 5

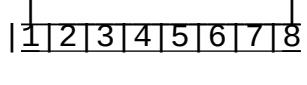
Table A2.5.3 DDS Instrument Set Point Data

Bit(s)	Measurement	Contents
1-8	EIT threshold, high level	0 to 255, commandable



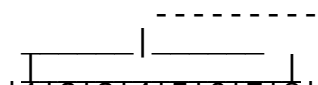
DDS set points 1 Byte 6

Bit(s)	Measurement	Contents
1-8	SEC threshold, low level	0 to 255, commandable



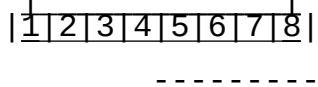
DDS set points 1 Byte 7

Bit(s)	Measurement	Contents
1-8	SEC threshold, high level	0 to 255, commandable



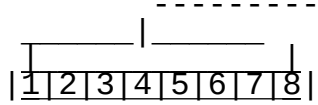
DDS set points 1 Byte 8

Bit(s)	Measurement	Contents
1-8	IN threshold, high level	0 to 255, commandable



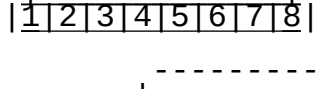
DDS set points 1 Byte 9

Bit(s)	Measurement	Contents
1-8	CN threshold, high level	0 to 255, commandable



DDS set points 1 Byte 10

Bit(s)	Measurement	Contents
1-8	EN threshold, high level	0 to 255, commandable



DDS set points 1 Byte 11

Bit(s)	Measurement	Contents
1-8	PN threshold, high level	0 to 255, commandable

DDS set points 1 Byte 12

Bit(s)	Measurement	Contents
1-8	PA threshold, low level	0 to 255, commandable

DDS set points 1 Byte 13

Bit(s)	Measurement	Contents
1-8	EA threshold, low level	0 to 255, commandable

DDS set points 1 Byte 14

Table A2.5.3 DDS Instrument Set Point Data

Bit(s)	Measurement	Contents	
1-8	CA threshold, low level	0 to 255, commandable	DDS set points 1 Byte 15
1-8	IA threshold, low level	0 to 255, commandable	DDS set points 2 Byte 1
1-8	HVC threshold, low level	0 to 255, commandable	DDS set points 2 Byte 2
1-8	CUR threshold, high level	0 to 255, commandable	DDS set points 2 Byte 3
1-8	spare		DDS set points 2 Byte 4
1-8	spare		DDS set points 2 Byte 5

A2.5.4 Digital Status and Analog Engineering. The content of the Digital Status and Analog Engineering section is shown in Table A2.5.4.

Table A2.5.4 Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-3	data frame number	000=A range science data 001=E range science data 010=set points 1 011=set points 2 100=auto test pulse 101=cmded test pulse 110=memory content 111=spare
4	mode 1:S/C sector data valid flag modes 2 & 3:spare	0=sector data not valid 1=sector data valid
5	mode 1:transmit status modes 2 & 3:spare	0=data not transmitted previously 1=data transmitted previously
6-8	mode 1:E range status modes 2 & 3:spares	E range science data 0-7

|1|2|3|4|5|6|7|8| DDS Byte 16

1-8	computer status	CPU status (CPU and memory check)

|1|2|3|4|5|6|7|8| DDS Byte 17

1-8	experiment current	15 to 100 ma.

|1|2|3|4|5|6|7|8| DDS Byte 18

1-8	HK channeltron high voltage	0 to 2500 volts

|1|2|3|4|5|6|7|8| DDS Byte 19

1-8	HK sensor ion grid high voltage	0 to -512 volts

|1|2|3|4|5|6|7|8| DDS Byte 20

1-8	HK +10 volts digital	0 to 15.36 volts

|1|2|3|4|5|6|7|8| DDS Byte 21

Table A2.5.4 Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents	
1-8	HK +7.5 volts analog	0 to 10 volts	DDS Byte 22
1-8	HK -7.5 volts analog	0 to -10 volts	DDS Byte 23
1-8	HK main electronics temperature	-30 degrees C to 80 degrees C	DDS Byte 24
1-8	commutated parity error, cmds acc, or cmd rej	see byte 26, bits 7-8	DDS Byte 25
1-6	synchronization word	101010 (binary)	DDS Byte 26
7-8	add-HK	determines whether byte 25 contains a parity error count, commands accepted, or commands rejected. 00=parity error count 01=cmds accepted count 10=cmds rejected count 11=spare	

A2.5.5 Telemetry Mode Changes. Upon the application of system power, DDS shall generate valid housekeeping data, but the science data shall not be valid.

Commanded telemetry mode changes shall be processed every RIM. Telemetry mode changes shall occur on RIM changes.

A2.6 ENERGETIC PARTICLE DETECTOR SUBSYSTEM TELEMETRY

This paragraph describes the format and content of the EPD output.

A2.6.1 EPD Packet. The schematic of this packet is shown in Figure A2.6.1. One EPD packet is inserted in each LPW/LNR Frame.

Title	Analog House-keeping	Digital Status	CMS PHA/ LEMMS PHA Data	LEMMS PHA Data	Rate Channel Data
Data Offset	0	8	72	168	208
Bits/packet	8	64	96	40	400
Description	A2.6.3	A2.6.4	A2.6.5	A.2.6.6	A2.6.7

Figure A2.6.1 EPD Packet

A2.6.1 Instrument Synchronicity. Within the EPD packet there will exist one major synchronism relative to the SCLK. The EPD Synchronization Index is equal to the SCLK Mod 91 count.

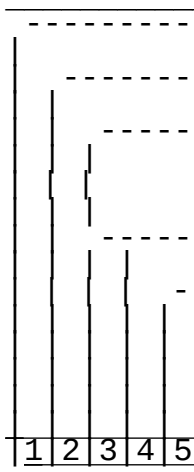
A2.6.3 Analog Housekeeping. The Analog Housekeeping section is one byte of subcommutated data. The contents of the subcommutated positions are shown in Table A2.6.1

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	spare	EPD Subcommutated Housekeeping S.I.=0
1-8	spare	EPD Subcommutated Housekeeping S.I.=1
1-8	motor housing temp.	EPD Subcommutated Housekeeping S.I.=2

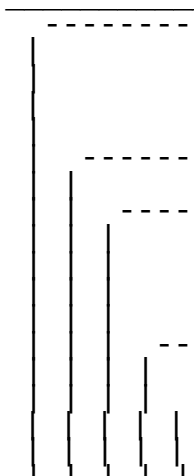
Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1	scan error	0=no error detected 1=error detected
2	fast scan abort flag	0=normal 1=fast scan aborted
3	emergency count flag	0=normal 1=means S.I.=3,bits 4-8 are now an emergency count number MOD 32
4	motor direction indicator	0=counter clockwise 1=clockwise
5	motor centerline indicator	0=motor not on enter-line 1=motor on centerline
6-8	motor position code	sector 0-7



EPD Subcommutated Housekeeping S.I.=3

Bit(s)	Measurement	Contents
1	emergency mode indicator	0=normal 1=emergency mode motor moves one step per trigger instead of one sector per trigger)
2	open loop mode indicator	0=closed loop 1=open loop
3	-in closed loop mode: modified scan -in open loop mode: limited scan	0=normal scan 1=modified scan 0=normal scan 1=limited scan
4	fast scan indicator	0=normal 1=fast scan
5	-in closed loop mode: go to sector N -in open loop mode: stop scanning after N triggers	0=normal 1=go to sector N, where N is value of S.I.=4, bits 6-8 0=normal 1=stop scanning after N triggers, where N is value if S.I.=4, bits 6-8
6-8	"N"	3 bit binary number



EPD Subcommutated Housekeeping S.I.=4

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

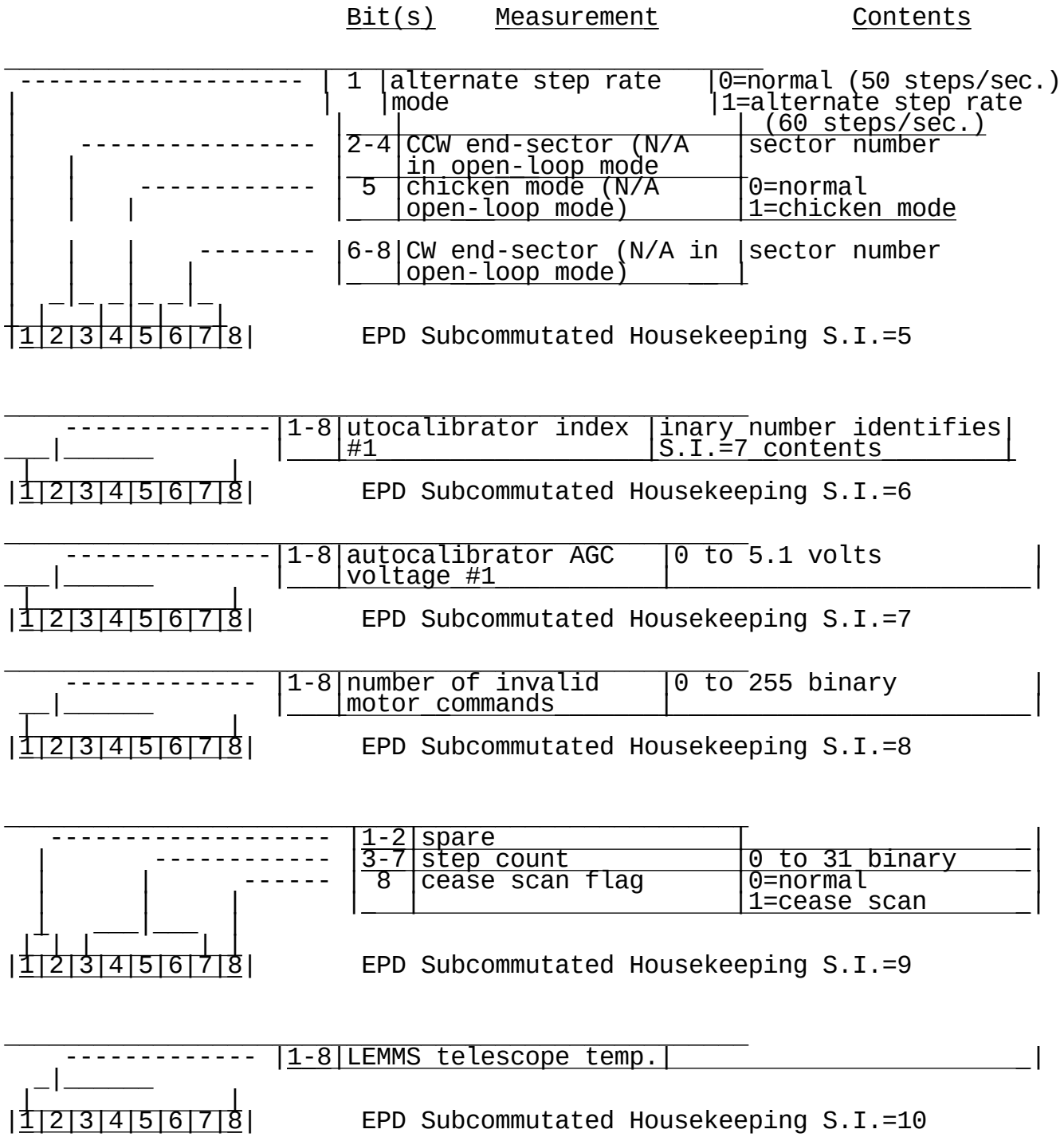


Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	number of invalid bus commands	0 to 255 binary

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=11

Bit(s)	Measurement	Contents
1-8	autocalibrator index # 2	binary number identifies S.I.=13 contents

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=12

Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage #2	0 to 5.1 volts

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=13

Bit(s)	Measurement	Contents
1-8	MSB memory dump cursor	8 MSB's of memory dump address

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=14

Bit(s)	Measurement	Contents
1-8	motor dwell period	motor dwell period in units of 1.333 sec.

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=15

Bit(s)	Measurement	Contents
1-8	CMS telescope temp.	

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=16

Bit(s)	Measurement	Contents
1-8	number of supervisory bus parity errors detected	0 to 255 binary

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=17

Bit(s)	Measurement	Contents
1-8	autocalibrator index # 3	binary number identifies S.I.=19 contents

1 2 3 4 5 6 7 8 — EPD Subcommutated Housekeeping S.I.=18

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage #3	0 to 5.1 volts

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=19

Bit(s)	Measurement	Contents
1-8	MSB upper memory checksum limit	8 MSB's of upper memory checksum limit

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=20

Bit(s)	Measurement	Contents
1-8	LSB upper memory checksum limit	8 LSB's of upper memory checksum limit

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=21

Bit(s)	Measurement	Contents
1-8	main elect. temp.	

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=22

Bit(s)	Measurement	Contents
1-8	memory checksum	

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=23

Bit(s)	Measurement	Contents
1-8	autocalibrator index # 4	binary number identifies S.I.=25 contents

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=24

Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage # 4	0 to 5.1 volts

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=25

Bit(s)	Measurement	Contents
1-8	MSB lower memory checksum limit	8 MSB's of lower memory checksum limit

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=26

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

	Bit(s)	Measurement	Contents
1 2 3 4 5 6 7 8	1-8	LSB lower memory checksum limit	8 LSB's of lower memory checksum limit
EPD Subcommutated Housekeeping S.I.=27			
1 2 3 4 5 6 7 8	1-8	EPD input current	
EPD Subcommutated Housekeeping S.I.=28			
1 2 3 4 5 6 7 8	1-8	number of supervisory bus parity errors detected during EPD bus transaction	0 to 255 binary
EPD Subcommutated Housekeeping S.I.=29			
1 2 3 4 5 6 7 8	1-8	autocalibrator index # 5	binary number identifies S.I.=31 contents
EPD Subcommutated Housekeeping S.I.=30			
1 2 3 4 5 6 7 8	1-8	autocalibrator AGC voltage # 5	0 to 5.1 volts
EPD Subcommutated Housekeeping S.I.=31			
1 2 3 4 5 6 7 8	1-8	spare	
EPD Subcommutated Housekeeping S.I.=32			
1 2 3 4 5 6 7 8	1-8	spare	
EPD Subcommutated Housekeeping S.I.=33			
1 2 3 4 5 6 7 8	1-8	+60 volts bias	
EPD Subcommutated Housekeeping S.I.=34			

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1	power switch status byte #1	0=LEMMS amp 8 (E2) off 1=LEMMS amp 8 (E2) on
2	power switch status byte #1	0=LEMMS amp 7 (D) off 1=LEMMS amp 7 (D) on
3	power switch status byte #1	0=LEMMS amp 6 (C) off 1=LEMMS amp 6 (C) on
4	power switch status byte #1	0=LEMMS amp 5 (E1)off 1=LEMMS amp 5 (E1) on
5	power switch status byte #1	0=LEMMS amp 4 (A)ff 1=LEMMS amp 4 (A) on
6	power switch status byte #1	0=LEMMS amp 3(F2) off 1=LEMMS amp 3 (F2) on
7	power switch status byte #1	0=LEMMS amp 2 (F1) off 1=LEMMS amp 2 (F1) on
8	power switch status byte #1	0=LEMMS amp 1 (B) off 1=LEMMS amp 1 (B) on

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=35

1-8	autocalibrator index # 6	binary number identifies S.I.=37 contents

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=36

1-8	autocalibrator index voltage #6	0 to 5.1 volts

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=37

1-8	spare	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=38

1-8	spare	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=39

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

	Bit(s)	Measurement	Contents
	1-8	Log amp. temperature	-171 to 69 deg. C
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=40	
	1	spare	
	2	power switch status byte #2	0=calibrator off 1=calibrator on
	3	power switch status byte #2	0=PHA off 1=PHA on
	4	power switch status byte #2	0=TOF off 1=TOF on
	5	power switch status byte #2	0=CMS electronics off 1=CMS electronics on
	6	power switch status byte #2	0=detector bias normal 1=detector bias high
	7	power switch status byte #2	0=TOVR RL off 1=TOVR RL on
	8	power switch status byte #2	0=LEMMS A detector bia off 1=LEMMS A detector bias on (+60 V)
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=41	
	1-8	autocalibrator index # 7	binary number identifies S.I.=43 contents
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=42	
	1-8	autocalibrator AGC voltage #7	0 to 5.1 volts
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=43	
	1-8	spare	
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=44	
	1-8	spare	
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=45	
	1-8	-15 volts power	
1 2 3 4 5 6 7 8		EPD Subcommutated Housekeeping S.I.=46	

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1	power switch status byte #3	0=LEMMS -10 V power off 1=LEMMS -10 V power on
2	power switch status byte #3	0=motor off 1=motor on
3	power switch status byte #3	0=motor RAM normal 1=motor RAM exchanged
4	power switch status byte #3	0=motor controller in normal mode 1=motor controller in memory load mode
5	power switch status byte #3	0=motor controller running 1=motor controller reset
6	spare	
7	power switch status byte #3	0=LEMMS E11 thresh. norm 1=LEMMS E11 thresh. high
8	power switch status byte #3	0=LEMMS A1 thresh. norm. 1=LEMMS A1 thresh. high

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=47

1-8	autocalibrator index # 8	binary number identifies S.I.=49 contents

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=48

1-8	autocalibrator AGC voltage #8	0 to 5.1 volts

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=49

1-8	upper alarm threshold for EPD input current	

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=50

1-8	lower alarm threshold for EPD input current	

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=51

1-8	+10 volts power	

|1|2|3|4|5|6|7|8| EPD Subcommutated Housekeeping S.I.=52

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

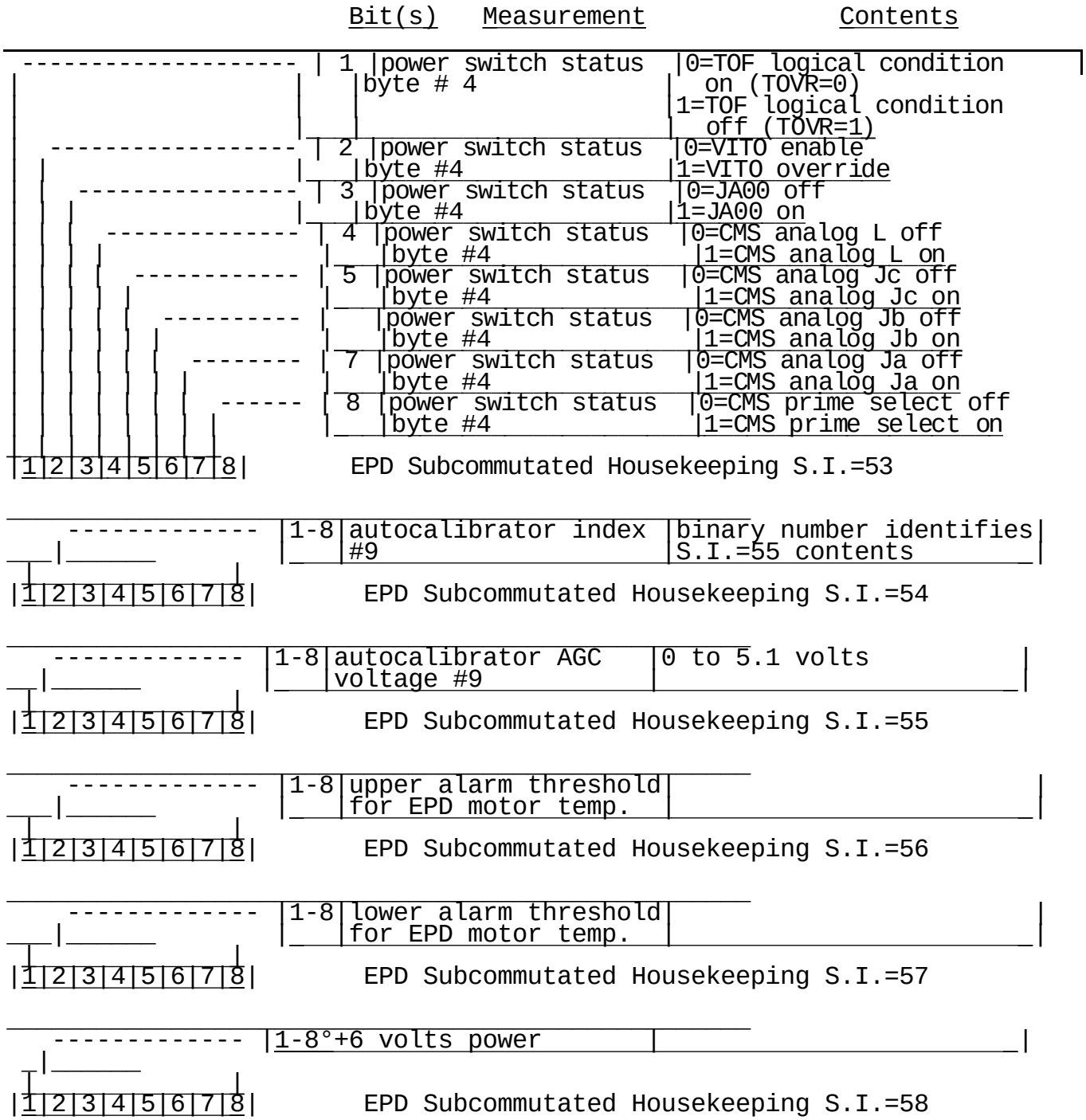


Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	spare	
EPD Subcommutated Housekeeping S.I.=59		
1-8	autocalibrator index #10	binary number identifies S.I.=61 contents
EPD Subcommutated Housekeeping S.I.=60		
1-8	autocalibrator index voltage #10	0 to 5.1 volts
EPD Subcommutated Housekeeping S.I.=61		
1-8	upper alarm threshold for LEMMS telescope temperature	
EPD Subcommutated Housekeeping S.I.=62		
1-8	lower alarm threshold for LEMMS telescope temperature	
EPD Subcommutated Housekeeping S.I.=63		
1-8	+3 volts power	
EPD Subcommutated Housekeeping S.I.=64		
1-7	spare	
8	Internal Monitor Status	0=Disabled 1=Enabled
EPD Subcommutated Housekeeping S.I.=65		
1-8	autocalibrator index #11	binary number identifies S.I.=67 contents
EPD Subcommutated Housekeeping S.I.=66		
1-8	autocalibrator AGC voltage #11	0 to 5.1 volts
EPD Subcommutated Housekeeping S.I.=67		

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	upper alarm threshold for CMS telescope temperature	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=68

Bit(s)	Measurement	Contents
1-8	lower alarm threshold for CMS telescope temperature	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=69

Bit(s)	Measurement	Contents
1-8	-3 volts power	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=70

Bit(s)	Measurement	Contents
1-8	spare	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=71

Bit(s)	Measurement	Contents
1-8	autocalibrator index #12	binary number identifies S.I.=73 contents

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=72

Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage #12	0 to 5.1 volts

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=73

Bit(s)	Measurement	Contents
1-8	upper alarm threshold for main electronics temperature	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=74

Bit(s)	Measurement	Contents
1-8	lower alarm threshold for main electronics temperature	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=75

Bit(s)	Measurement	Contents
1-8	-6 volts power	

1	2	3	4	5	6	7	8

EPD Subcommutated Housekeeping S.I.=76

Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	spare	

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=77

Bit(s)	Measurement	Contents
1-8	autocalibrator index #13	binary number identifies S.I.=79 contents

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=78

Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage #13	0 to 5.1 volts

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=79

Bit(s)	Measurement	Contents
1-8	upper alarm threshold + 10 volts power	

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=80

Bit(s)	Measurement	Contents
1-8	lower alarm threshold + 10 volts power	

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=81

Bit(s)	Measurement	Contents
1-8	-10 volts power	

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=82

Bit(s)	Measurement	Contents
1-8	spare	

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=83

Bit(s)	Measurement	Contents
1-8	autocalibrator index #14	binary number identifies S.I.=85 contents

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=84

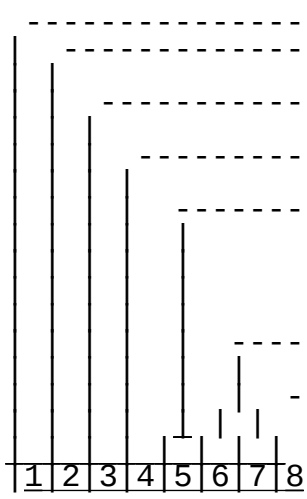
Bit(s)	Measurement	Contents
1-8	autocalibrator AGC voltage #14	0 to 5.1 volts

|1|2|3|4|5|6|7|8|

EPD Subcommutated Housekeeping S.I.=85

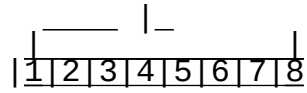
Table A2.6.1 Subcommutated Analog Housekeeping (bit 1 is MSB)

Bit(s)	Measurement	Contents
1	spare	
2	PHA control byte output clear	0=PHA output clear 1=PHA output normal
3	PHA control byte override	0=priority normal 1=priority override
4	PHA control byte reset	0=PHA normal 1=PHA reset
5-6	PHA control byte lemms flavor/priority	2 bit LEMMS select 0=A,1=E, 2=F (orif bit 3=1, then this determines priority, 0=I, 1=II, 2=III, 3=IV)
7	PHA control byte read active	0=P read active 1=P read inactive
8	PHA control byte mode	0=LEMMS mode 1=CMS mode



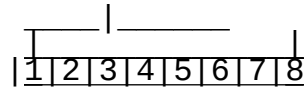
EPD Subcommutated Housekeeping S.I.=86

1-8	spare	



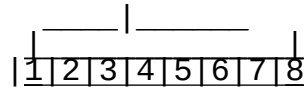
EPD Subcommutated Housekeeping S.I.=87

1-8	spare	



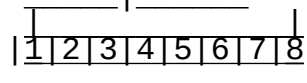
EPD Subcommutated Housekeeping S.I.=88

1-8	spare	



EPD Subcommutated Housekeeping S.I.=89

1-8	spare	



EPD Subcommutated Housekeeping S.I.=90

A2.6.4 Digital Status. The contents of the Digital Status section is described in Table A2.6.2.

Table A2.6.2 Digital Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1	scan error	0=no error detected 1=error detected
2	fast scan abort flag	0=normal 1=fast scan aborted
3	emergency count flag	0=normal 1=means byte 2 bits 4-8 are now an mergency count number MOD 32
4	motor direction indicator	0=counter clockwise 1=clockwise
5	motor centerline indicator	0=motor not on center-line 1=motor on centerline
6-8	motor position code	Sector 0-7

|1|2|3|4|5|6|7|8| EPD Byte #2

1-8	memory dump	8 bits of memory

|1|2|3|4|5|6|7|8| EPD Byte #3

1-8	memory dump cursor	8 LSB's of memory dump address (8 MSB are in subcommutated data, 16 bits total)

|1|2|3|4|5|6|7|8| EPD Byte #4

1-8	commands executed	number of commands executed MOD 256 since last power on.

|1|2|3|4|5|6|7|8| EPD Byte #5

1-8	packet parity	exclusive-OR of all other bytes in packet

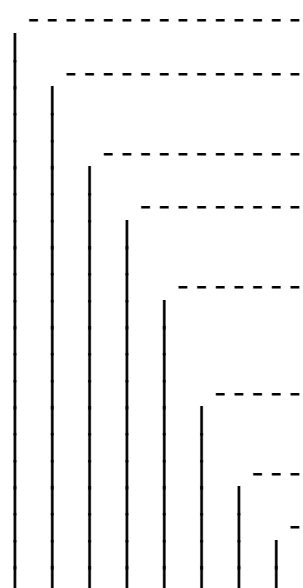
|1|2|3|4|5|6|7|8| EPD Byte #6

1-8	command op code	operation code of last command executed

|1|2|3|4|5|6|7|8| EPD Byte #7

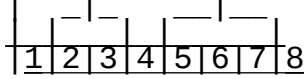
Table A2.6.2 Digital Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1	alternating mode	0=normal CMS mode 1=CMS alternating mode
2	power monitor flag	0=normal 1=EPD power recently interrupted
3	bus adaptor parity error flag	0=normal 1=parity error detected
4	Resynchronization flag	0=normal 1=EPD recently resynced to CDS
5	cease scan flag	0=normal 1=motor controller has entered "cease scan" mode
6	motor in motion flag	0=normal 1=motor was in motion during this packet
7	singles/background flag	0=S/B format L 1=S/B formats J or J'
8	J/J' indicator	0=CMS mode J 1=CMS mode J'



EPD Byte #8

Bit(s)	Measurement	Contents
1	Modulo 2 counter	0=even packet 1=odd packet
2-4	Modulo 7 counter	increments every packet
5-8	Modulo 13 counter	increments when Mod 7 counter resets*



EPD Byte #9

* [7(MOD 13)+(MOD 7)+2] modulo91=SCLK Mod 91

A2.6.5 CMS PHA/LEMMS PHA Data. The contents of the CMS PHA/LEMMS PHA Data section can be either CMS PHA data or LEMMS PHA data. The timing of when the data is CMS PHA or LEMMS PHA is shown in Table A2.6.3

Table A2.6.3 SI vs. CMS PHA/
LEMMS PHA section contents

MOD 91	Contents
2	LEMMS PHA data
9	LEMMS PHA data
16	LEMMS PHA data
23	LEMMS PHA data
30	LEMMS PHA data
37	LEMMS PHA data
44	LEMMS PHA data
51	LEMMS PHA data
58	LEMMS PHA data
65	LEMMS PHA data
72	LEMMS PHA data
79	LEMMS PHA data
86	LEMMS PHA data
All Others	CMS PHA data

The CMS PHA data section contains information on Composition Measurement System (CMS) Pulse Height Analyzer (PHA) data. LEMMS PHA data contains information on Low Energy Magnetospheric Measurement System (LEMMS) PHA spectrum data. When this section contains CMS PHA data, the contents are described in Table A2.6.4, which refers to one event.

Thirteen times throughout one major frame (i.e., when the MOD 91 counter registers 2, 9, 16, 23, 30, 37, 44, 51, 58, 65, 72, 79, and 86) the 12 bytes (96 bits) of CMS PHA data will be replaced by LEMMS PHA data. The 12 bytes, in addition to the 35 bytes of LEMMS PHA found in bits 169 to 208 of each of the 7 packets of EPD telemetry form one complete 47-byte LEMMS PHA spectrum. The 47 byte LEMMS PHA spectrum will be sorted into energy bins (or bin numbers), which are given in Table A2.6.6.

Table A2.6.4 CMS PHA Data (bit 1 is MSB)

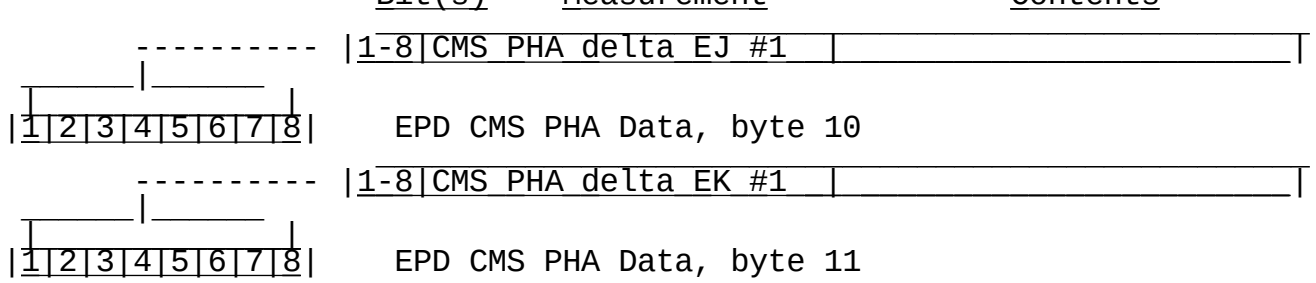


Table A2.6.4 CMS PHA Data (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-8	CMS PHA TOF #1	
	EPD CMS PHA Data, byte 12	
1-2	J ID #1	0=Jc 1=Jb 2=N/A 3=Ja
3-4	last transmitted priority #1	0=priority 1 1=priority 2 2=priority 3 3=priority 4
5-8	CMS PHA rate channel code #1	0=CM5 1=CN0 2=CN1 3=CH5 4=CH2 5=CH3 6=CH4 7=N/A 8=CM2 9=CM3 10=CM4 11=N/A 12=C ALPHA 2 13=C ALPHA 3 14=C ALPHA 4 15=N/A
	EPD CMS PHA Data, byte 13	
1-8	CMS PHA delta EJ #2	
	EPD CMS PHA Data, byte 14	
1-8	CMS PHA delta EK #2	
	EPD CMS PHA Data, byte 15	
1-8	CMS PHA TOF #2	
	EPD CMS PHA Data, byte 16	

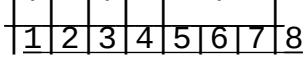
Table A2.6.4 CMS PHA Data (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-2	J ID #2	0=Jc 1=Jb 2=N/A 3=Ja
3-4	last transmitted priority #2	0=priority 1 1=priority 2 2=priority 3 3=priority 4
5-8	CMS PHA rate channel code #2	0=CM5 1=CN0 2=CN1 3=CH5 4=CH2 5=CH3 6=CH4 7=N/A 8=CM2 9=CM3 10=CM4 11=N/A 12=C ALPHA 2 13=C ALPHA 3 14=C ALPHA 4 15=N/A

1	2	3	4	5	6	7	8	
								EPD CMS PHA Data, byte 17
1-8								CMS PHA delta EJ #3
								EPD CMS PHA Data, byte 18
1-8								CMS PHA delta EK #3
								EPD CMS PHA Data, byte 19
1-8								CMS PHA TOF #3
								EPD CMS PHA Data, byte 20

Table A2.6.4 CMS PHA Data (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-2	J ID #3	0=Jc 1=Jb 2=N/A 3=Ja
3-4	last transmitted priority #3	0=priority 1 1=priority 2 2=priority 3 3=priority 4
5-8	CMS PHA rate channel code #3	0=CM5 1=CN0 2=CN1 3=CH5 4=CH2 5=CH3 6=CH4 7=N/A 8=CM2 9=CM3 10=CM4 11=N/A 12=C ALPHA 2 13=C ALPHA 3 14=C ALPHA 4 15=N/A

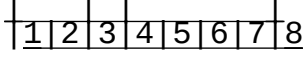


EPD CMS PHA Data, byte 21

A2.6.6 LEMMS PHA Data. The LEMMS PHA data section contains an additional 5 (8 bit) bytes of LEMMS PHA data. The contents of this section is shown in Table A2.6.5.

Table A2.6.5 LEMMS PHA Data (bit 1 is MSB)

Bit(s)	Measurement	Contents
1-3	LEMMS PHA spectrum element #1 exponent	if exponent=7, then value=mantissa, if not, value=$(\text{mantissa}+32)\cdot 2^{\text{exp}}$
4-8	LEMMS PHA spectrum element #1 mantissa	



EPD LEMMS PHA Data, byte 22

Table A2.6.5 LEMMS PHA Data (bit 1 is MSB)

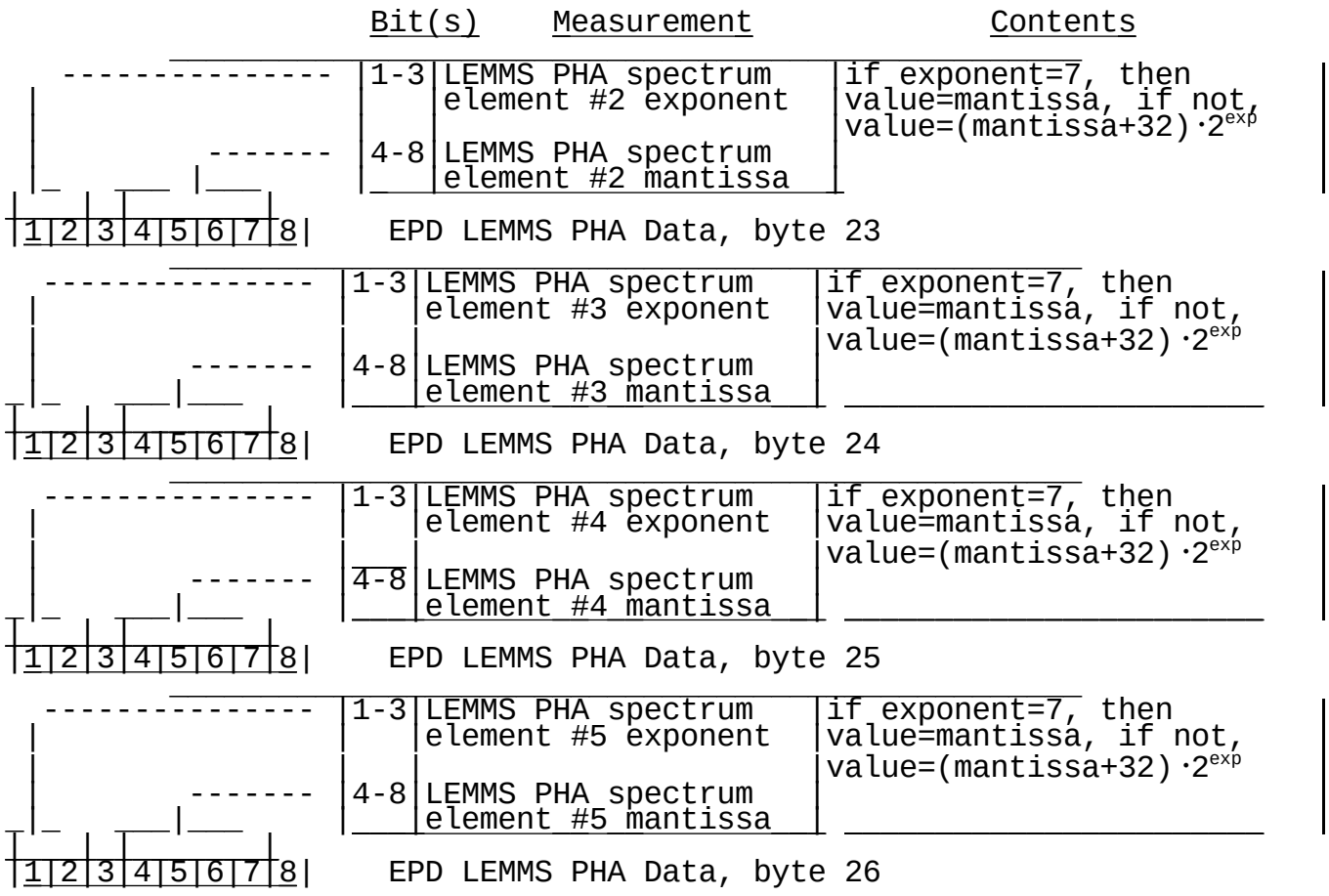


Table A2.6.6. GALILEO EPD LEMMS PHA Bin Assignments

Packet Identifier (Modulo 7 counter)	Byte Number	LEMMS PHA Bin Number
0	10	1
0	11	2
0	12	3
0	13	4
0	14	5
0	15	6
0	16	7
0	17	8
0	18	9
0	19	10
0	20	11
0	21	12
0	22	13
0	23	14
0	24	15
0	25	16
0	26	17
1	22	18
1	23	19
1	24	20
1	25	21
1	26	22
2	22	23
2	23	24
2	24	25
2	25	26
2	26	27
3	22	28
3	23	29
3	24	30
3	25	31
3	26	32
4	22	33
4	23	34
4	24	35
4	25	36
4	26	37
5	22	38
5	23	39
5	24	40
5	25	41
5	26	42
6	22	43
6	23	44
6	24	45
6	25	46
6	26	47

A2.6.7 Rate Channel Data. The Rate Channel Data section contains 40 rate channels, 10 bits each, of CMS and LEMMS sensor data. The particular rate channel involved depends on the Mod 2 counter described in Table A2.6.2. Table A2.6.7 shows the contents of the Rate Channel section for odd and even packets.

EPD rate channel accumulators are 10 bits log compressed from 24 bits. The log compression algorithm can be stated as follows:

Given a 24 bit binary integer with MSB on the left and LSB on the right, find the most significant "1". The number of bits to the right of the most significant "1", minus six, is the exponent. If this exponent value is negative, or if the original number itself is zero, set the exponent to 15, and use the six least significant bits of the original 24 bit number as the mantissa. If this is not the case, use the six bits immediately to the right of the most significant "1" as the mantissa.

The log decompression algorithm can be stated as follows:

Given the 10 bit log compressed rate channel data, the first 4 bits are the exponent, and the last 6 bits are the mantissa. If the exponent = 15, then the value = mantissa; if not then the value = (mantissa + 64) $\cdot 2^{exp}$.

Table A2.6.7 EPD Rate Channel Data

Bits	Even Packet[1]			Odd Packet[2]		
	CMS J	LEMMS	CMS J'	CMS J S/B J	LEMMS S/B L	CMS J' S/B J'
209-218		E01			E03	
219-228		E11			E13	
229-238		A01			A03	
239-248		A11			A13	
249-258		A21			A22	
259-268		E21			E22	
269-278		E31			E32	
279-288		F01			F02	
289-298		F11			F12	
299-308		A31			A32	
309-318		A41			A42	
319-328		A51			A52	
329-338		A61			A62	
339-348		A71			A72	
349-358		F21			F22	
359-368		F31			F32	
369-378	CE2		CE2P	CM3		CM3P
379-388	CE3		CE3P	CM4		CM4P
389-398	CE1		CE1P	CM5		CM5P
399-408	CP1		CP1P	CN1		CN1P
409-418		E02			EO4	
419-428		E12			E14	
429-438		A02			AO4	
439-448		A12			A14	
449-458	CP2		CP2P	CH2		CH2P
459-468	CP3		CP3P	CH3		CH3P
469-478	CH0		CH0P	CH4		CH4P
479-488	CH1		CH1P	CH5		CH5P
489-498		A81		EB1	KS	KP
499-508		DC0		EB2	JB	EB2
509-518		DC1		FB2	FB1	FB1
519-528		DC2		AS	AS	AS
529-538		DC3		CA0		CA0P
539-548		B01		CA2		CA2P
549-558		B11		BS	LS	BS
559-568		B21		CS	JA	JAP
569-578	CA1		CA1P	CM0		CM0P
579-588	CA3		CA3P	CM2		CM2P
589-598	CA4		CA4P	CN0		CN0P
599-608	CM1		CM1P	DS	JC	JCP

NOTES:

1. If the LEMMS column is blank, use the CMS J column if the J/J' indicator is zero, otherwise use the CMS J' column.
2. If the LEMMS S/B L column is blank, treat as in footnote 1. If all three columns contain names, this is a Singles/Background channel. Use the LEMMS S/B L column if the Singles/Background Flag is zero, otherwise treat the same as in footnote 1.

A2.6A HEAVY ION COUNTER SUBSYSTEM TELEMETRY

These paragraphs describe the format and content of the HIC output.

A2.6A.1 HIC Packet. The schematic of the HIC packet is shown in Figure A2.6A.1. 3 LPW/LNR Frames are required to transport 1 HIC Packet.

Title	1st Rate Area	1st Tag Word	1st PHA Area	1st CRC Word	2nd Rate Area	2nd Tag Word	2nd PHA Area	2nd CRC Word	3rd Rate Area	Status Word	3rd Tag Word	3rd PHA Area	3rd CRC Word
Data Offset	0	36	48	84	96	132	144	180	192	216	228	240	276
Bits/Packet	36	12	36	12	36	12	36	12	24	12	12	36	12
Description	A2.6A.3	A2.6A.4	A2.6A.5	A2.6A.6	A2.6A.3	A2.6A.4	A2.6A.5	A2.6A.6	A2.6A.3	A2.6A.7	A2.6A.4	A2.6A.5	A2.6A.6

A2.6A.1 HIC Packet

A2.6A.2 Instrument Synchronicity. There are 30 1/3 packets per RIM. The HIC Packet can start in any LPW/LNR frame. HIC Packet synchronization is achieved by searching for a 1, 2, 3, 12, 13, or 14 in the 4 MSB of the 3rd word of any HIC allocation. This would identify a status word.

The Synchronization Index is the first 4 bits of the status word (see Table A2.6A.7). The Synchronization Index applies to the subcommutated Rate Channels, and the subcommutated status word.

A2.6A.3 Rate Channel Sections 1, 2, and 3. These three sections contain 12 bit log compressed rate channel data. The first section contains three (3) rate channels, as shown in Table A2.6A.1.

Table A2.6A.1 Rate Channel Section 1

Word	Rate Channel
1	DUBL, Double Event - detectors LE1 and LE2 in LET E telescope
2	TRPL, Triple Event - detectors LE1, LE2, and LE3 in LET E telescope
3	WDSTP, Wide Stopping Event - detectors LE2, LE3, and LE4 in LET E telescope

The second section contains three (3) rate channels, as shown in Table A2.6A.2.

Table A2.6A.2 Rate Channel Section 2

Word	Rate Channel
1	WDPEN, Wide Penetrating Event - detectors LE2, LE3, LE4 and LE5 in LET E telescope
2	LETB, Any Event in LET B telescope
3	LE 1, Any Firing of the LE Detector in LET E telescope

The third section contains two (2) subcommutated rate channels, as shown in Table A2.6A.3.

Table A2.6A.3 Subcommutated Rate Channel Section

S.I.	1st. Word LE Singles	2nd. Word LB Singles
0	SB	SLB
1	SB	SLB
2	SB	SLB
3	SB	LBTRP
4	SB	SLB
5	SB	SLB
6	SB	SLB
7	SB	SLB
8	LE5	LB1
9	LE3	LB2
10	LE4	LB3
11	LE2	LB4
12	SB	SLB
13	SB	SLB
14	SB	SLB
15	SB	SLB

The acronyms used in Table A2.6A.3 are defined as follows:

SB	An event triggering the slant discriminators in telescope LET E.
SLB	An event triggering the slant discriminators in telescope LET B.
LBTRP	An event triggering the first 3 detectors in the LET B telescope.
LE (n)	Any triggering of detector (n) in the LET E telescope.
LB (n)	Any triggering of detector (n) in the LET B telescope.

The algorithms for the rate channel data compression and reconstruction are shown in Figure A2.6A.2.

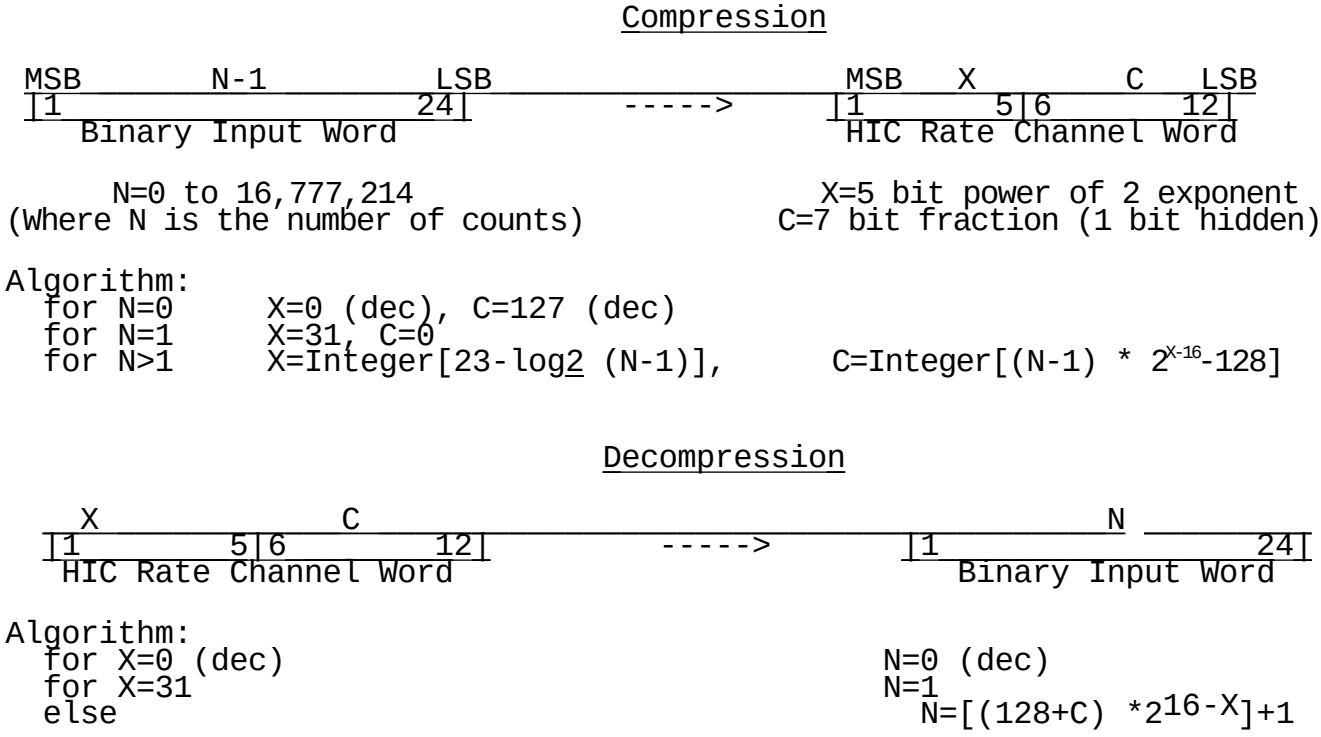


Figure A2.6A.2. Rate channel compression/decompression algorithm.

A2.6A.4 PHA Areas 1, 2, and 3. These three sections contain unsigned 12 bit numbers representing single sizes from various detectors. Eachsection contains three (3) 12 bit words. the contents of each word are determined by the tag word described in paragraph A2.6A.5. Each tag word describes the immediately preceding PHA Area. Table A2.6A.4 describes the contents of these areas.

Table A2.6A.4 PHA Words

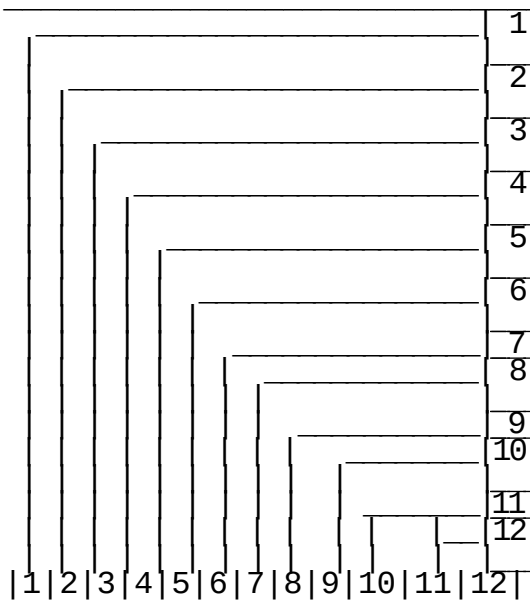
Word	Contents*	
	LET E telescope	LET B telescope
1	PHA 3 - LE3	LB3
2	PHA 2 - LE1, if bit 1 of Tag word=0 (LE4+LE5) if bit 1 of Tag word=1	LB2
3	PHA 1 - LE2	LB1

*Note - if no event is available, all zero's are telemetered.

A2.6A.5 Tag Word 1, 2, and 3. The tag words describe the contents of the PHA Areas described above. Bit 9 of the Tag words describes whether the data was from the LET E or LET B telescope. Table A2.6A.5 describes the tag word contents for the LET E telescope, and Table A2.6A.6 describes the Tag word contents for the LET B telescope.

Table A2.6A.5 HIC Tag Word (MSB is Bit 1) for LET E (Bit 9=0)

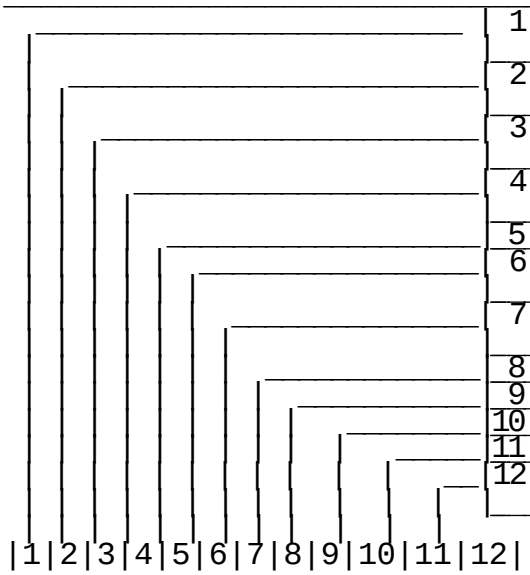
Bit(s)	Measurement	Contents
1	LE4 discriminator	0=disc. did not fire 1=disc. did fire
2	LE1 discriminator	0=disc. did not fire 1=disc. did fire
3	LE5 discriminator	0=disc. did not fire 1=disc. did fire
4	LE3 discriminator	0=disc. did not fire 1=disc. did fire
5	SB discriminator	0=disc. did not fire 1=disc. did fire
6	LE2 discriminator	0=disc. did not fire 1=disc. did fire
7	spare	0
8	High Gain status	0=normal, low gain 1=high gain
9	LET E/LET B	0 (LET E)
10	DUBL mode	0=not in double mode 1=in double mode
11	block ID	1 (not used)
12	caution flag	0=good event 1=compromised event



Tag word for LET E telescope

Table A2.6A.6 HIC Tag Word (MSB is Bit 1) for LET B (Bit 9=1)

Bit(s)	Measurement	Contents
1	SLB discriminator	0=disc. did not fire 1=disc. did fire
2	LB3 discriminator	0=disc. did not fire 1=disc. did fire
3	LB2 discriminator	0=disc. did not fire 1=disc. did fire
4	LB1 discriminator	0=disc. did not fire 1=disc. did fire
5	spare	0
6	LB2 terms	0=normal 1=term deleted
7	LB3 terms	0=normal 1=term deleted
8	spare	0
9	LET E/LET B	1 (LET B)
10	spare	0
11	block ID	1=not used
12	caution flag	0=good event 1=compromised event



Tag word for LET B telescope

A2.6A.6 CRC Words 1, 2, and 3. The CRC words are a cyclic Redundancy check over the 84 bits preceding each word. The first 8 bits contain the CRC word, with the last four bits fixed as zero's. The algorithm used for the checksum is shown in Figure A2.6A.3.

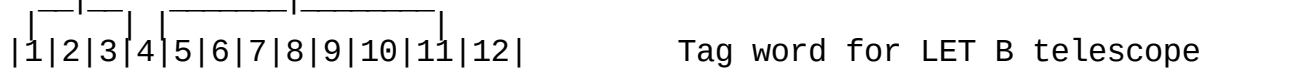
```
initialize 84-element array x() to zero
loop for n = 1 to 84
        input = nth bit of 84-bit data stream
        x(0) = x(8) XOR input
        x(8) = x(7) XOR x(0)
        x(7) = x(6) XOR x(0)
        x(6) = x(5)
        x(5) = x(4)
        x(4) = x(3)
        x(3) = x(2)
        x(2) = x(1)
        x(1) = x(0)
        end of loop
        CRC = 128*x(8) + 64*x(7) + 32*x(6) + 16*x(5) + 8*x(4) +
              4*x(3) + 2*x(2) + x(1)
```

Figure A2.6A.3 CRC Algorithm

A2.6A.7 Status Word. The contents of the status word is shown in Table A2.6A.7

Table A2.6A.7 Digital Status (Bit 1 is MSB)

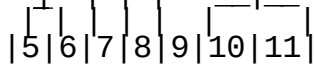
Bit(s)	Measurements	Contents
1-4	synchronization index	0-15 (dec)
5-12	subcommutated status	see Tables A2.6A.8 to A2.6A.13



The subcommutated status is valid only for the Synchronization Index equaling 0, 2, 6, 8, 12, and 13. The contents are shown in Tables A2.6A.8 through A2.6A.13 respectively.

Table A2.6A.8 Subcommutated Status (SI=0)

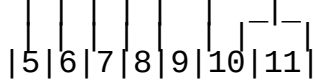
Bit(s)	Measurement	Contents
5-6	not used	0
7	High Voltage Enable Status	0=high voltage off 1=high voltage on
8	High Gain status	0=normal gain 1=high gain
9	not used	
10-12	Calibration status	000=cal off,or 1st state 001=2nd state 010=3rd state 011=4th state 100=5th state 101=6th state 110=7th state 111=8th state



subcommutated status for S.I.=0

Table A2.6A.9 Subcommutated Status (SI=2)

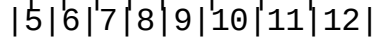
Bit(s)	Measurement	Contents
5	LE1 Pre-AMP Power Status	0=Power on 1=Power off
6	LE2 Pre-Amp Power Status	0=Power on 1=Power off
7	LE3 Pre-Amp Power Status	0=Power on 1=Power off
8	LE4 Pre-Amp Power Status	0=Power on 1=Power off
9	not used	
10	LE5 Pre-Amp Power Status	0=Power on 1=Power off
11-12	not used	



subcommutated status for S.I.=2

Table A2.6A.10 Subcommutated Status (SI=6)

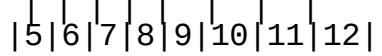
Bit(s)	Measurement	Contents
5-6	not used	0
7	WDSTP mode	0=normal 1=mode deleted
8	TRPL mode	0=normal 1=mode deleted
9	not used	0=normal 1=mode deleted
10	DUBL mode	0=normal 1=mode deleted
11	LET B	0=normal 1=mode deleted
12	WDPEN mode	0=normal 1=mode deleted



subcommutated status for S.I.=6

Table A2.6A.11 Subcommutated Status (SI=8)

Bit(s)	Measurement	Contents
5	LB3 terms	0=normal 1=term deleted
6	LB2 terms	0=normal 1=term deleted
7	not used	0
8	LE3 terms	0=normal 1=term deleted
9	LE4 terms	0=normal 1=term deleted
10	LE1/B2 terms	0=normal 1=term deleted
11	LE2/B1 terms	0=normal 1=term deleted
12	LE1/A2 terms	0=normal 1=term deleted



subcommutated status for S.I.=8

Table A2.6A.12 Subcommutated Status (SI=12)

Bit(s)	Measurements	Contents
5-8	not used	0
9	LB4 Pre-amp Power Status	0=power on 1=power off
10	LB3 Pre-amp Power Status	0=power on 1=power off
11	LB2 Pre-amp Power Status	0=power on 1=power off
12	LB1 Pre-amp Power Status	0=power on 1=power off

|5|6|7|8|9|10|11|12| subcommutated status for S.I.=12

Table A2.6A.13 Subcommutated Status (SI=13)

Bit(s)	Measurements	Contents
5	redundant High Voltage command received	0=command not received 1=command received
6	Cal/Stim disable	0=normal 1=disabled
7-10	not used	0
11	Auto Gain command	0=auto gain not commanded 1=auto gain commanded
12	High Gain command	0=high gain not commanded 1=high gain commanded

|5|6|7|8| 9|10|11|12| subcommutated status for S.I.=13

A2.6A.8 Telemetry Mode Changes. Upon application of system power, the HIC shall configure itself to a state where only status telemetry is valid.

Commanded telemetry mode changes are processed once per minor frame. Mode changes will occur at the next RTI.

A2.6B EXTREME ULTRAVIOLET SUBSYSTEM TELEMETRY. These paragraphs describe the format and content of the EUV output.

A2.6B.1 EUV Spin Packet. The Galileo EUV spin packet is described in Table A2.6B.1.

A2.6B.2 Data System. The digital output shall consist of 12-8 bit words per telemetry request (minor frame). The word formats are described in the following sections. The data rate shall be 144 bits per second.

A2.6B.2.1 Digital Status. The first twelve bytes requested from the EUV by CDS at the start of each major frame shall consist of a fixed format packet of digital status. (see table A2.6B.2)

A2.6B.2.1.1 Synchronization Pattern. The first two bytes of the digital status packet are a fixed pattern meant to give a 'synchronization' pattern should the microprocessor lose spacecraft time. This pattern is defined to be 7E (hex). (Chosen because the pixel at 7E is not used, so address data will never be 7E).

A2.6B.2.1.2 Discrete Digital Status Byte. This byte shall indicate the current mode of the EUV Channel. It uses one bit to indicate the current mode, three bits for the High Voltage control, or four status bits. Table A2.6B.2 describes this byte in more detail. This byte shall be a reflection of the most recently issued EUV Channel Command Signals.

A2.6B.2.1.3 RIM Counter. These three bytes shall indicate the current major frame (RIM) counter. Its purpose here is to make the EUV telemetry packet self contained.

A2.6B.2.1.4 Sector Size Status. This byte should be a copy of the commanded sector size. It indicates the number of 20.8 millisecond periods per sector.

A2.6B.2.1.5 Number of Sectors Per Integration Period. This byte should be a copy of the commanded number of sectors.

A2.6B.2.1.6 Software Accumulators. Two separate buffers, each 16 bits wide, shall be updated internal to the EUV instrument. The first buffer contains registers for each of the sectors in the commanded mode. Each of these registers are incremented whenever a photon of any wavelength is detected within each sector. The second buffer contains 128 registers for each of the 128 pixels, and each register will be incremented whenever a photon is detected by its associated pixel, regardless of the sector. (See Figure A2.6B.1).

A2.6B.2.1.6.1 Sector Accumulator Address. This is the address of the sector being read out in the next two bytes. This address will be set to zero whenever the EUV receives a new command. Otherwise it will simply roll modulo the commanded number of sectors.

A2.6B.2.1.6.2 Sector Accumulator Data. These two bytes are the number of photons accumulated in the sector addressed in the Sector Accumulator Address. These registers are cleared only upon microprocessor initialization.

A2.6B.2.1.6.3 Wavelength Integrator Address. This is the address of the next Pixel (wavelength) to be read out. Note that the actual integration bytes are part of the spin packet which occurs approximately three times per major frame, thus allowing the sector accumulator readout to more closely match the wavelength readout (Nominally there will be 25 or less sectors). These registers are also cleared only at microprocessor initialization.

A2.6B.2.2 Spin Packets. The spin packets shall contain an 'FE' Hex sync pattern, two bytes of wavelength integration data, and two bytes containing the minor frame (MOD91) counter and RTI (MOD10) counter in which integration started for this revolution. These will be followed by a variable number of pixel address bytes indicating a photon has been detected in that particular pixel and sector.

A2.6B.2.2.1 Wavelength Integration Data. The second and third bytes of a Spin Packet contain the high order, then the low order, of the 16 bit accumulated data for the current pixel (as defined in the digital housekeeping packet).

A2.6B.2.2.2 Spin Integration Start Time. The fourth and fifth bytes of each spin packet contain the minor frame (MOD91) counter and RTI (MOD10) counter respectively, during which integration started on this revolution.

A2.6B.2.2.3 Pixel Address Information. In order to meet telemetry bandwidths, it has been decided to send the 7 bit address information down whenever a pixel detects a photon or background count. See Table A2.6B.1 for a description and discussion relating to the Spin Packets.

Table A2.6B.1. EUV Spin Packets Description

* / Bit \ Byte	MSB 1	2	3	4	5	6	7	8
1	0	1	1	1	1	1	1	0
2	0	1	1	1	1	1	1	0
3	FAST MUX	FLAG	126 BUFFER	SPIN	1	1	1	1	0
4	RIM Counter MSByte								
5	RIM Counter								
6	RIM Counter LSByte								
7	Sector Size								
8	Number of Sectors								
9	Sector Accumulator Address								
	OVERFL								

10	Sector Accumulator Data (MSByte)
11	Sector Accumulator Data (LSByte)
12	Wavelength Integration Address

Table A2.6B.2. EUV Housekeeping TLM Format Descriptions

Byte	Bit (s) *	Description
1,2	1 - 8	Fiducial - These will each be 7E hex.
3	1	Fast Mux Mode 0 = Normal 1 step/RIM 1 = Fast Mux 1 step/4 minor frames
3	2	126 Flag - indicates whether pixel 126 has been active during the preceding major frame 0 = inactive 1 = active
3	3	Spin Buffer Overflow - indicates if data has been lost in the preceding major frame due to high count rates. 0 = no overflow 1 = overflow (data lost)
3	4	127 Flag - indicates whether pixel 127 has been active during the preceding frame. 0 = inactive 1 = active
3	5	EUV Channel Mode 0 = Pulse Integration Mode 1 = Pulse Counting Mode
3	6 - 8	EUV High Voltage Control 000 = High Voltage Off 001 - 111 = Discrete HV Steps
4	1 - 8	RIM Counter (MSByte) - This is a copy of the upper 8 bits of the 24 bit RIM Counter. It is included here to make the EUV TM Data self contained.
5	1 - 8	RIM Counter - This is the middle 8 bits of the 24 bit RIM Counter.
6	1 - 8	RIM Counter - This is the lower 8 bits of the 24 bit RIM Counter.
7	1 - 8	Sector Size - Indicates the number of 20.8 milliseconds period for each sector.
8	1 - 6	Number of Sectors - Indicates the number of sectors before integration starts.

Table A2.6B.2. EUV Housekeeping TLM Format Descriptions

Byte	Bit (s) *	Description
9	1 - 8	Sector Integrator Address - Indicates the sector address of the Sector Data that follows in the next two bytes.
10,11	1 - 8	Sector Integrator Data - The accumulated number of photons of any detected wavelength in this sector since the last read-out. Byte 10 will be the µs byte.
12	1 - 8	Wavelength Integrator Address - Indicates wavelength address (pixel) of the integrate wavelength data that follows in the next spin packet.

*Bit numbering conventions are per GLL-3-290.

A2.7 MAGNETOMETER SUBSYSTEM TELEMETRY

These paragraphs describe the format and content of the output of the Magnetometer Subsystem.

A2.7.1 MAG Packet. The schematic of a MAG Packet is shown in Figure A2.7.1. One packet is placed in each LPW/LNR frame.

Title	Instrument Status	1st Science Sample	2nd Science Sample	3rd Science Sample
Data Offset	0	16	64	112
Bits/packet	16	48	48	48
Description	A2.7.3	A2.7.4	A2.7.5	A2.7.6

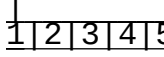
Figure A2.7.1 MAG Packet

A2.7.2 Instrument Synchronicity. The contents of the MAG Packet can be uniquely determined from the data within the packet and the SCLK Mod 91 count. The MAG Synchronization Index is equal to the SCLK Mod 91 count.

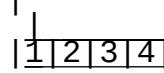
A2.7.3 Instrument Status. The contents of the Instrument Status section are two bytes of subcommutated analog and digital status values. This is shown in Table A2.7.1. The positions are shown relative to synchronization index in Table A2.7.2.

Table A2.7.1 Instrument Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	Most significant 8 bits of subcommutated instrument status data.	8 MSB's of subcommutated data
1-8	Least significant 8 bits of subcommutated instrument status data.	8 LSB's of subcommutated data



MAG Byte #1



MAG Byte #2

Table A2.7.2 Instrument Status Subcommutated Data

SI	MEASUREMENT	CONTENTS
0	Current Scale Factor	0000000000000010= Inboard sensor high (±16 KnT) 0000000001000000= Inboard sensor low or Outboard sensor high (±512 nT) 0000100000000000=Outboardsensor low (±16 nT) ALL OTHERS ARE N/A
1	MAG select and gain select	0101XXXXXXXXXXX(*)= Outboard sensor on 1010XXXXXXXXXXX= Outboard sensor off XXXXXXXX0101XXXX= Inboard sensor on XXXXXXXX1010XXXX= Inboard sensor off XXXX0101XXXXXXXX= Outboard sensor gain high XXXX1010XXXXXXXX= Outboard sensor gain low XXXXXXXXXXXX0101=Inboard sensor gain high XXXXXXXXXXXX1010=Inboard sensor gain low ALL OTHERS ARE N/A
2	Current flip positions	11100001XXXXXXXX=Outboard sensor flipped right 00011110XXXXXXXX=Outboard sensor flipped left XXXXXXXX11100001=Inboard sensor flipped right

		XXXXXXXX00011110=Inboard sensor
		flipped left
		ALL OTHERS ARE N/A
3	Last flip command	11100001XXXXXXXX= Outboard sensor
		commanded right
		00011110XXXXXXXX= Outboard sensor
		commanded left
		XXXXXXXX11100001= Inboard sensor
		commanded right
		XXXXXXXX00011110= Inboard sensor
		commanded left
		ALL OTHERS ARE N/A

(*) where X is irrelevent

Table A2.7.2 Instrument Status Subcommutated Data

SI	MEASUREMENT	CONTENTS
4	Calibrate enable/flip power on	XXXXXXXX01010101= Calibrate
	power enable	XXXXXXXX10101010= Calibrate power off
		00001000XXXXXXXX= Flipper power on (start, flipper power decrements from 1000 to 0000. A step occurs at every MOD 91 count)
		00000000XXXXXXXX= Flipper power off
		ALL OTHERS ARE N/A
5	Gain 1	-2 to +1.999939
6	Gain 2	-2 to +1.999939
7	Gain 3	-2 to +1.999939
8	Offset 1	Field Units
9	Offset 2	Field Units
10	Offset 3	Field Units
11	Rotation 11	-1 to +0.9999695
12	Rotation 12	-1 to +0.9999695
13	Rotation 13	-1 to +0.9999695
14	Rotation 21	-1 to +0.9999695
15	Rotation 22	-1 to +0.9999695
16	Rotation 23	-1 to +0.9999695
17	Rotation 31	-1 to +0.9999695
18	Rotation 32	-1 to +0.9999695
19	Rotation 33	-1 to +0.9999695
20	Despin status	01010101XXXXXXXX= Despin on
		10101010XXXXXXXX= Despin off
		ALL OTHERS ARE N/A
21	S/C time	16 MSB's of RIM
22	S/C time	8 LSB of RIM, and MOD 91 count
23	Spin angle	spin angle as received from CDS
24	Spin delta angle	spin delta as received from CDS
25	X at 21	Field Units

26	Y DSPIN at 21	Field Units
27	Z DSPIN at 21	Field Units
28	Calibration coil	01010101XXXXXXXX= on 10101010XXXXXXXX= off ALL OTHERS ARE N/A
29	Optimal averager/ snapshot data status	01010101XXXXXXXX= Optimal averager on 10101010XXXXXXXX= Optimal averager off XXXXXXXX01010101= Snapshot data on XXXXXXXX10101010= Snapshot data off ALL OTHERS ARE N/A
30	Memory keep alive volt	-20 V. to +19.9993900 V
31	+12 Volts DC	-20 V. to +19.9993900 V
32	+10 Volts DC	-20 V. to +19.9993900 V
33	-12 Volts DC	-20 V. to +19.9993900 V

Table A2.7.2 Instrument Status Subcommutated Data

SI	MEASUREMENT	CONTENTS
34	Reference V+	-20 V. to +19.9993900 V
35	Reference Gnd	-5 V. to +5 V.
36	Temperature Electronics	-5 V. to +4.9998475 V.
37	+V - clip	-5 V. to +4.9998475 V.
38	-V - clip	-5 V. to +4.9998475 V.
39	Parity error counters	MSByte=H/W, LSByte=S/W
40	XNF	Field Units
41	YNF	Field Units
42	ZNF	Field Units
43	spare	
44	spare	
45	spare	
46	DSP-Constant	
47	Aver #	
48	spare	
49	spare	
50	X aver	Field Units
51	X^{O} Sin 0 aver	Field Units
52	X^{O} Cos 0 aver	Field Units
53	Y^{O} aver	Field Units
54	Y^{O} Sin 0 aver	Field Units
55	Y^{O} Cos 0 aver	Field Units
56	Z^{O} aver	Field Units
57	Z^{O} Sin 0 aver	Field Units

^{O}

58	Z Cos 0 aver	Field Units
59	spare	
60	ROM checksum pointer	0 to 4000
61	ROM checksum	LSByte=0 to 255
62	RAM checksum pointer	16384 to 20480
63	RAM checksum	LSByte=0 to 255
64	ROM CKSUM (POR)	CKSUM $0000 - $0FFF
65	RAM CKSUM (POR)	CKSUM $4000 - $46FF
66	S/C time	16 MSB's of RIM
67	S/C time	8 LSB of RIM, and MOD 91 count
68	Spin angle	spin angle as received from CDS
69	Spin delta angle	spin delta as received from CDS
70	X aver at 66	Field Units
71	Y aver at 66	Field Units
72	Z aver at 66	Field Units
73	Data buffer beginning address	4800 (HEX) to 4D00 (HEX)
74	Data buffer	Field Units
75	Data buffer	Field Units

Table A2.7.2 Instrument Status Subcommutated Data

SI	MEASUREMENT	CONTENTS
76	Data buffer	Field Units
77	Data buffer	Field Units
78	Data buffer	Field Units
79	Data buffer	Field Units
80	Data buffer	Field Units
81	Data buffer	Field Units
82	Data buffer	Field Units
83	Data buffer	Field Units
84	Data buffer	Field Units
85	Data buffer	Field Units
86	Data buffer	Field Units
87	Data buffer	Field Units
88	Data buffer	Field Units
89	Data buffer	Field Units
90	Command counter	Set to zero at each POR

A.2.7.3.1 Data Buffer Format. The data provided in the OPTIMAL AVERAGING, and SNAPSHOT modes of the magnetometer is stored in a data buffer provided between locations 4800-4D00. This data includes the current storage pointer, start time, sector data and 200 vector samples of the magnetic field in the OPTIMAL AVERAGER MODE. In the SNAPSHOT mode, the data is stored in reverse order due to timing restrictions in the interrupt handling routines, and includes the start time and 210 vector samples. Format details are provided in Table A.2.7.3. This data is read out in 16 16-bit blocks once each M0D91 frame from address 4800-4D00 and placed in the magnetometer subcommutated data from SI=74 through SI=89. (see Table A.2.7.2). In order to collect one complete buffer of data, approximately 40 frames must be read. The data readout continuously cycles between addresses 4800-4D00.

Table A2.7.3 MAG DATA BUFFER CONTENT

OPTIMAL AVERAGER		SNAPSHOT	
Memory Location		Memory Location	
4800	8 MSB of X @ T o	4800	8 LSB Sensor 3 data @ T 209
4801	8 LSB of X @ T o	4801	8 MSB Sensor 3 data @ T 209
4802	8 MSB of Y @ T o	4802	8 LSB Sensor 2 data @ T 209
4803	8 LSB of Y @ T o	4803	8 MSB Sensor 2 data @ T 209
4804	8 MSB of Z @ T o	4804	8 LSB Sensor 1 data @ T 209
4805	8 LSB of Z @ T o	4805	8 MSB Sensor 1 data @ T 209
.	.	.	.
.	.	.	.
.	.	.	.
4CAA	8 MSB of X @ T 199	4CE6	8 LSB Sensor 3 data @ T o
4CAB	8 LSB of X @ T 199	4CE7	8 MSB Sensor 3 data @ T o
4CAC	8 MSB of Y @ T 199	4CE8	8 LSB Sensor 2 data @ T o
4CAD	8 LSB of Y @ T 199	4CE9	8 MSB Sensor 2 data @ T o
4CAE	8 MSB of Z @ T 199	4CEA	8 LSB Sensor 1 data @ T o
4CAF	8 LSB of Z @ T 199	4CEB	8 MSB Sensor 1 data @ T o

4CC4 Current storage pointer	4CF1 16 MSB of RIM (SCLK)
4CFO 16 MSB of RIM (SCLK)	4CF3 8 LSB of RIM and MOD91
4CF2 8 MSB of RIM and MOD91	
4CF4 S/C Sector Data	

In the "Optimal Average" mode timing between vectors is controlled by the AVERAGE # found in SI47 of the instrument status data. The timing is always a multiple of the MOD91 timing and is defined by

DELTA T = (AVERAGE # + 1) *60.6666

In the "Snap Shot" mode timing between vectors is 33.3 ms or 30 vectors per second.

A2.7.4 1st Science Sample. The 1st Science Sample section contains 3 (16 bit) samples of sensor data collected exactly 1 MOD 91 count prior to the SCLK MOD 91 count of the LPW/LNR frame they are within. The 3 (16 bit) samples are 3 measurements corresponding to the X, Y, and Z axis, respectively. The measurements are output in field units, which can be converted to nano-teslas (nT) by dividing by the scale value provided in the instrument status (SI=0, Table A2.7.2).

$Field_{nT}$ = ($Field_{FU}$)/SCALE (*)

(*) SCALE shall be commandable to a selected value.

Each sample is a 16 bit two's complement word which ranges from -32768 to +32767

A2.7.5 2nd Science Sample. The 2nd Science Sample section contains 3 (16 bit) samples of sensor data collected at 222.22 ms after the MOD 91 count prior to the SCLK MOD 91 count of the LPW/LNR frame they are within. The 3 (16 bit) samples are 3 measurements corresponding to the X, Y, and Z axis, respectively. The measurements are output in field units, which can be converted to nano-teslas (nT) by dividing by the scale value provided in the instrument status (SI=0, Table A2.7.2).

$Field_{nT}$ = ($Field_{FU}$)/SCALE

Each sample is a 16 bit two's complement word which ranges from -32768 to +32767

A2.7.6 3rd Science Sample. The 3rd Science Sample section contains 3 (16 bit) samples of sensor data collected at 444.44 ms after the MOD 91 count prior to the SCLK MOD 91 count of the LPW/LNR frame they are within. The 3 (16 bit) samples are 3 measurements corresponding to the X, Y, and Z axis, respectively. The measurements are output in field units, which can be converted to nano-teslas (nT) by dividing by the scale value provided in the instrument status (SI=0, Table A2.7.2).

$Field_{nT}$ = ($Field_{FU}$)/SCALE

Each sample is a 16 bit two's complement word which ranges from -32768 to +32767

A2.7.7 Telemetry Mode Changes. Upon the application of system power, MAG shall automatically configure itself to a standby mode. MAG data packets will contain no valid data in this mode.

Commanded telemetry mode changes are processed every RIM.

A2.8 NEAR INFRARED MAPPING SPECTROMETER SUBSYSTEM TELEMETRY

This paragraph describes the format and content of the NIMS output.

A2.8.1 NIMS Low Rate Science Packet. The schematic of the NIMS Low Rate Science packet is shown in Figure A2.8.1. One NIMS packet is placed in each LPW/LNR frame.

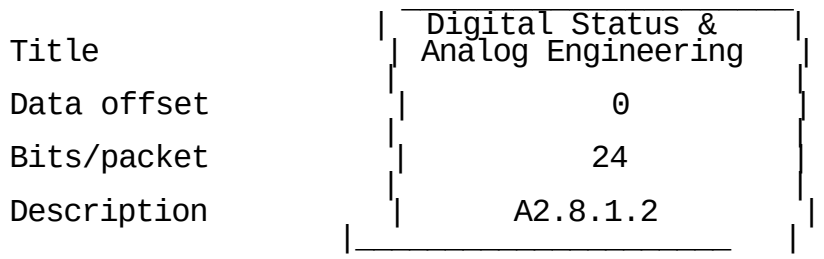


Figure A2.8.1 NIMS LPW/LNR Packet

A2.8.1.1 Instrument Synchronicity. There will exist one major synchronism for the NIMS data output within the LPW/LNR frame. The Synchronization Index will be equal to the SCLK MOD 91 count.

A2.8.1.2 LRS Digital Status & Analog Engineering. The LPW/LNR Digital Status & Analog Engineering section is 3 bytes of subcommutated data. Table A2.8.1 gives the contents of each NIMS housekeeping word, and Table A2.8.2 gives the subcommutated positions of each of the housekeeping words. All subcommutated positions not explicitly called out and described are spares. As an example, Word #1 (mode repeat count) is described in Table A2.8.1. The position of the word in the NIMS LPW/LNR packet is (shown in Table A2.8.2) Byte 1, and occurs when the MOD 91 count is 0.

Table A2.8.1 LPW/LNR Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	mode repeat count: PTAB 1	# of times to repeat this table before switching to PTAB 2

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 1

1	mirror operation bit: PTAB 1	1=mirror is scanning 0=mirror is fixed
2	autobias operation bit: PTAB 1	1=autobias off 0=autobias on
3-8	grating start position: PTAB 1	

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 2

Table A2.8.1 LRS (LPW/LNR) Digital Status & Analog Engineering (MSB is bit 1)

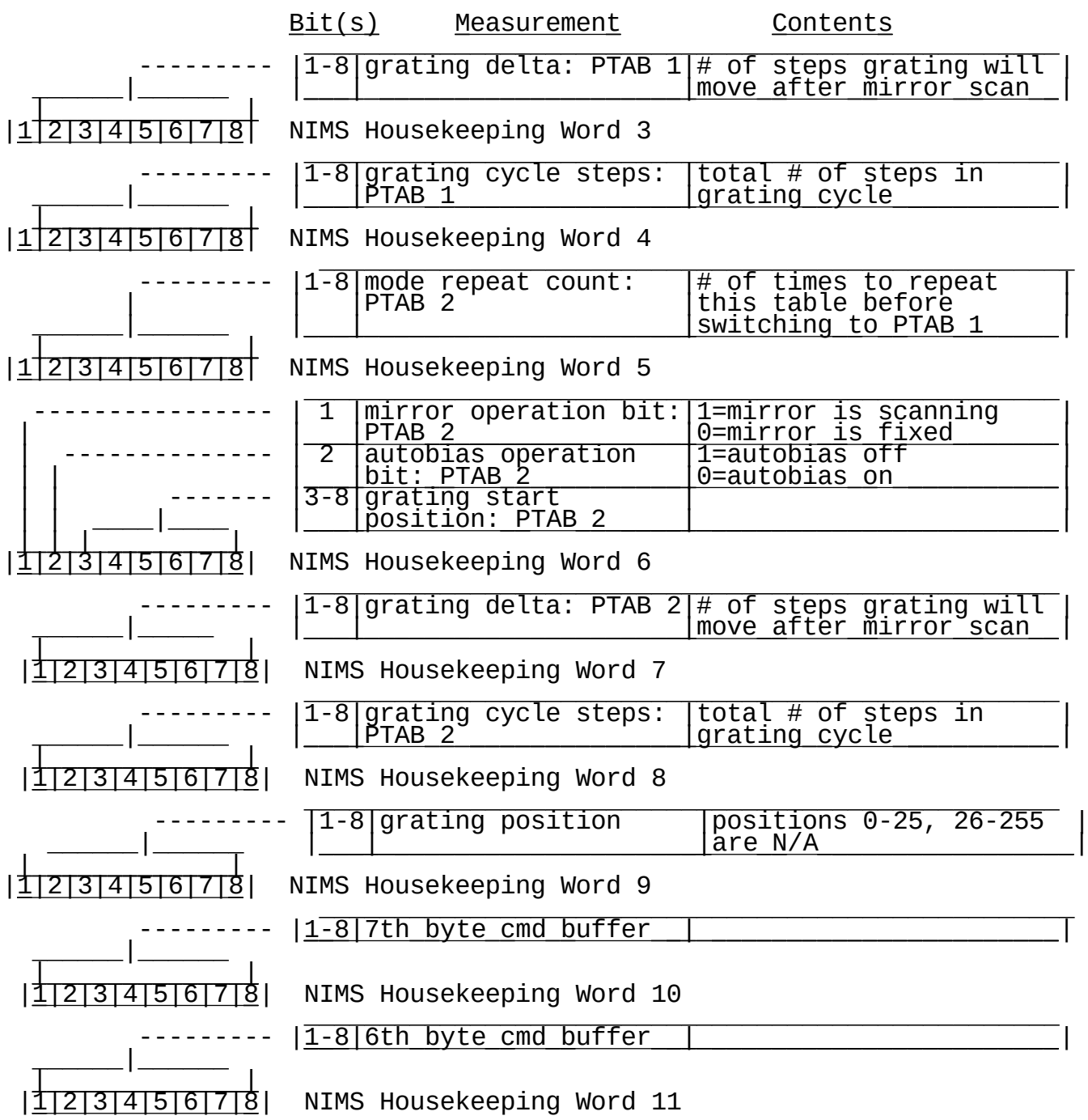


Table A2.8.1 LRS (LPW/LNR) Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents	
1-8	5th byte cmd buffer		1|2|3|4|5|6|7|8 NIMS Housekeeping Word 12
1-8	4th byte cmd buffer		1|2|3|4|5|6|7|8 NIMS Housekeeping Word 13
1-8	3rd byte cmd buffer		1|2|3|4|5|6|7|8 NIMS Housekeeping Word 14
1-8	2nd byte cmd buffer		1|2|3|4|5|6|7|8 NIMS Housekeeping Word 15
1-8	LS byte cmd buffer		1|2|3|4|5|6|7|8 NIMS Housekeeping Word 16
1-8	NIMS Xaction parity error	count of bus parity errors in transaction	1|2|3|4|5|6|7|8 NIMS Housekeeping Word 17
1-8	Bus parity error	count of all bus parity errors	1|2|3|4|5|6|7|8 NIMS Housekeeping Word 18
1-8	power supply input I	0 to 400 ma	1|2|3|4|5|6|7|8 NIMS Housekeeping Word 19
1-8	ave mirror drive I	0 to 200 ma	1|2|3|4|5|6|7|8 NIMS Housekeeping Word 20
1-8	ave grating drive I	0 to 200 ma	1|2|3|4|5|6|7|8 NIMS Housekeeping Word 21

Table A2.8.1 LRS (LPW/LNR) Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	reference voltage	0 to 24 volts

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 22

1	h/w parity error in cmd or S/C time hdr	0=no error detected 1=error detected
2	memory location status	0=ROM 1=RAM
3-4	gain state	00=gain 2 01=gain 4 10=gain 3 11=gain 1
5	electronics calibrate	0=cal off 1=cal on
6	optics cal status	0=cal lamp off 1=cal lamp on
7-8	chopper status	00=chopper on, synchron. 01=chopper on, synchron. 10=chopper off 11=chopper on, free run

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 23

1	parity error in S/C time data	0=no error detected 1=error detected
2	parity error in command data	0=no error detected 1=error detected
3	chopper synchronization	0=chopper in sync with RTI 1=chopper not in sync with RTI
4	ADC/MUX error	0=operation normal 1=operation not completed in allotted time
5	formatter error	0=operation normal completed in allotted time
6	MOD 91 count error	0=no error detected 1=transmitted MOD 91 count does not equal the internal MOD 91 count
7	MOD 10 count error	0=no error detected 1=transmitted MOD 10 count does not equal the

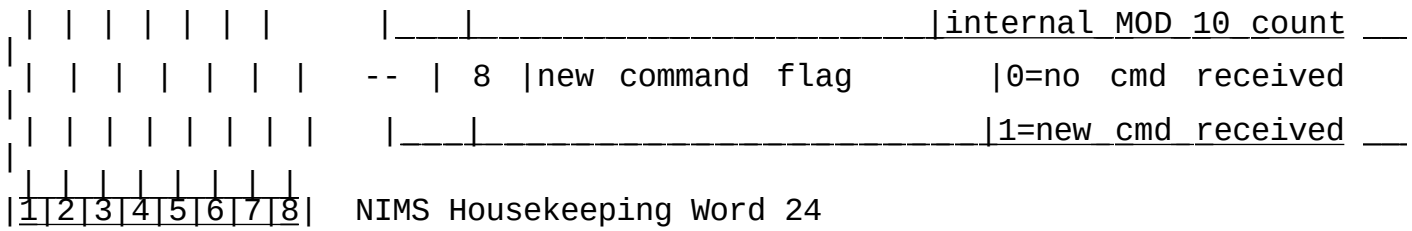

-- 8 new command flag
0=no cmd received
1=new cmd received
internal MOD 10 count
1 2 3 4 5 6 7 8
NIMS Housekeeping Word 24

Table A2.8.1 LRS (LPW/LNR) Digital Status & Analog Engineering (MSB is bit 1)

	Bit(s)	Measurement	Contents
NIMS Housekeeping Word 25	1	current PTAB	0=PTAB 1 1=PTAB 2
	2-8	spare	
NIMS Housekeeping Word 26	1-8	optics cal source I	0 to 100 ma
NIMS Housekeeping Word 27	1-6	spares	
	7-8	Si channel MS byte	
NIMS Housekeeping Word 28	1-8	Si channel LS byte	
NIMS Housekeeping Word 29	1-6	spares	
	7-8	InSb channel MS byte	
NIMS Housekeeping Word 30	1-8	InSb channel LS byte	
NIMS Housekeeping Word 31	1-8	check sum	ROM check sum

Table A2.8.2 NIMS LRS (LPW/LNR) Housekeeping Word Subcommutated Positions

Subcommutated Positions		
Word #	Byte	MOD 91
1	1	0
2	2	0
3	3	0
4	1	1
5	2	1
6	3	1
7	1	2
8	2	2
9	3	2, 5-90
10	1	3
11	2	3
12	3	3
13	1	4
14	2	4
15	3	4
16	1	5
17	2	5
18	2	6
19	1	7
20	2	7
21	1	8
22	2	8
23	1	10
24	2	10
25	2	11-65, 68-90
26	1	16
27	1	66
28	2	66
29	1	67
30	2	67
31	1	90

A2.8.2 NIMS High Rate Data Packet. The schematic of this packet is shown in Figure A2.8.2. At data rates of 28.8 kbps and 115.2 kbps, one NIMS high rate packet is placed in each frame of TDM telemetry data (one frame every MOD 10 count). At data rates of 403.2 kbps and 806.4 kbps, one NIMS high rate packet is divided equally among 8 successive TDM telemetry frames (one frame every MOD 8 count).

High-rate NIMS data is also placed into the 7.68 Kbps LNR & LPU TDM telemetry formats. Both of these inclusions (22.5% of full HRS NIMS stream) for LNR and (53.5% of full HRS NIMS stream) for LPU are CDS-editted and compacted before being placed in their respective telemetry formats; the edit/compaction process is one that varies according to command driven instructions to the CDS.

Title	Digital Status & Analog Engineering	Background	Sensor Data
Data offset	0	48	88
Bits/packet	48	40	680
Description	A2.8.2.2	A2.8.2.3	A2.8.2.4

Figure A2.8.2 NIMS High Rate Data Packet

A2.8.2.1 Instrument Synchronicity. The NIMS high rate data is synchronized only on a MOD 10 and MOD 91 basis.

A2.8.2.2 HRS Digital Status & Analog Engineering. The HRS Digital Status & Analog Engineering section consists of 6 bytes of subcommutated data. Table A2.8.3 gives the contents of each NIMS housekeeping word, and Table A2.8.4 gives the subcommutated positions of each of the housekeeping words. All subcommutated positions not explicitly called out and described are spares. As an example, Word #1 (mode repeat count) is described in Table A2.8.3. The position of the word in the NIMS High rate packet is (shown in Table A2.8.4) Byte 3, and occurs when the MOD 91 count is 0 through 90, and the MOD 10 count is 1, and again when the MOD 10 count is 6.

Table A2.8.3 HRS Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	mode repeat count: current PTAB	# of times to repeat this table
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 1	
1	mirror operation bit	1=mirror is scanning 0=mirror is fixed
2	autobias operation bit	1=autobias off 0=autobias on
3-8	grating start position	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 2	
1-8	grating delta	# of steps grating will move after mirror scan
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 3	
1-8	grating cycle steps	total # of steps in grating cycle
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 4	
1-8	grating position	positions 0-25, 26-255 are N/A
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 5	
1-8	mirror position	positions 0-19, 20-255 are N/A
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 6	
1-8	7th byte cmd buffer	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 7	

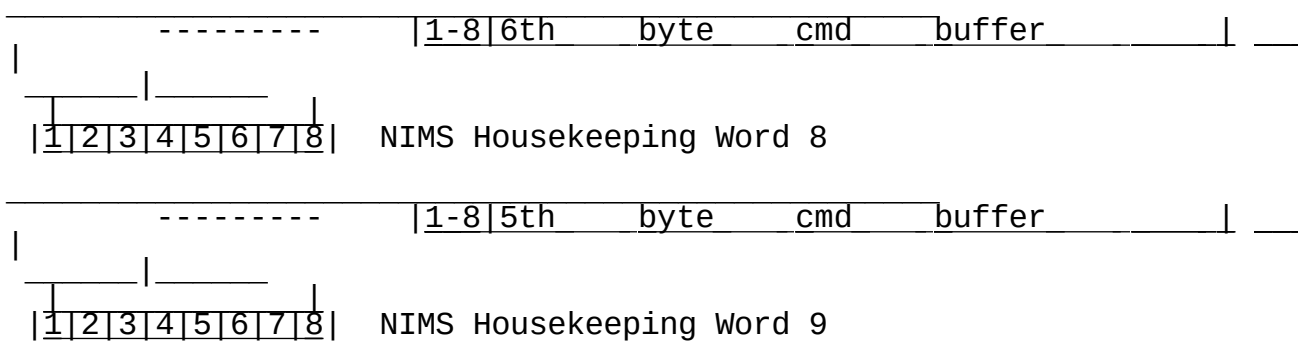

1-8 6th byte cmd buffer
1 2 3 4 5 6 7 8
NIMS Housekeeping Word 8
1-8 5th byte cmd buffer
1 2 3 4 5 6 7 8
NIMS Housekeeping Word 9

Table A2.8.3 HRS Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	4th byte cmd buffer	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 10	
1-8	3rd byte cmd buffer	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 11	
1-8	2nd byte cmd buffer	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 12	
1-8	LS byte cmd buffer	
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 13	
1	h/w parity error in cmd or S/C time hdr	0=no error detected 1=error detected
2	memory location status	0=ROM 1=RAM
3-4	gain state	00=gain 2 01=gain 4 10=gain 3 11=gain 1
5	electronics calibrate	0=cal off 1=cal on
6	optics cal status	0=cal lamp off 1=cal lamp on
7-8	chopper status	00=chopper on, synchron. 01=chopper on, synchron. 10=chopper off 11=chopper on, free run
1 2 3 4 5 6 7 8	NIMS Housekeeping Word 14	

Table A2.8.3 HRS Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1	parity error in S/C time data	0=no error detected 1=error detected
2	parity error in command data	0=no error detected 1=error detected
3	chopper synchronization RTI	0=chopper in sync with RTI 1=chopper not in sync with RTI
4	ADC/MUX error	0=operation normal 1=operation not completed in allotted time
5	formatter error	0=operation normal 1=operation not completed in allotted time
6	MOD 91 count error	0=no error detected 1=transmitted MOD 91 count does not equal the internal MOD 91 count
7	MOD 10 count error	0=no error detected 1=transmitted MOD 10 count does not equal the internal MOD 10 count
8	new command flag	0=no cmd received 1=new_cmd_received

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 15

1-8	NIMS Xaction parity error	count of bus parity errors in transaction

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 16

1-8	Bus parity error	count of all bus parity errors

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 17

1-8	power supply input I	0 to 400 ma

|1|2|3|4|5|6|7|8| NIMS Housekeeping Word 18

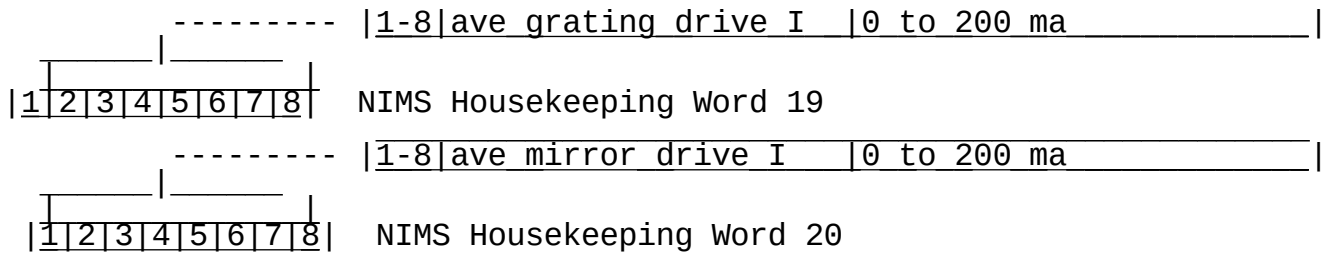

1-8|ave grating drive I |0 to 200 ma
1|2|3|4|5|6|7|8|
NIMS Housekeeping Word 19
1-8|ave mirror drive I |0 to 200 ma
1|2|3|4|5|6|7|8|
NIMS Housekeeping Word 20

Table A2.8.3 HRS Digital Status & Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	reference voltage	0 to 24 volts
1|2|3|4|5|6|7|8	NIMS Housekeeping Word 21	
1-8	optics cal source I	0 to 100 ma
1|2|3|4|5|6|7|8	NIMS Housekeeping Word 22	
1-8	check sum	ROM check sum
1|2|3|4|5|6|7|8	NIMS Housekeeping Word 23	

Table A2.8.4 NIMS Housekeeping Word Subcommutated Positions

	Subcommutated Positions		
Word #	Byte	MOD 91	MOD 10
1	3	0-90	1,6
2	4	0-90	1,6
3	5	0-90	1,6
4	6	0-90	1,6
5	1	0-90	1,6
6	2	0-90	1,6
7	1	0	8
8	2	0	8
9	3	0	8
10	4	0	8
11	5	0	8
12	6	0	8
13	6	0	9
14	5	1	8
15	6	1	8
16	6	2	8
17	6	4	8
18	6	8	8
19	5	16	8
20	6	16	8
21	6	32	8
22	6	48	8
23	6	64	8

A2.8.2.3 Background Data. The contents of the Background data section consist of 5 bytes of background infrared science data. These 5 bytes comprise 4 (10 bit) words, as shown in Table A2.8.5. The background data from the 17 NIMS detectors are commutated into the Background data section as shown in Table A2.8.6.

Table A2.8.5 NIMS Background Data (MSB is bit 1)

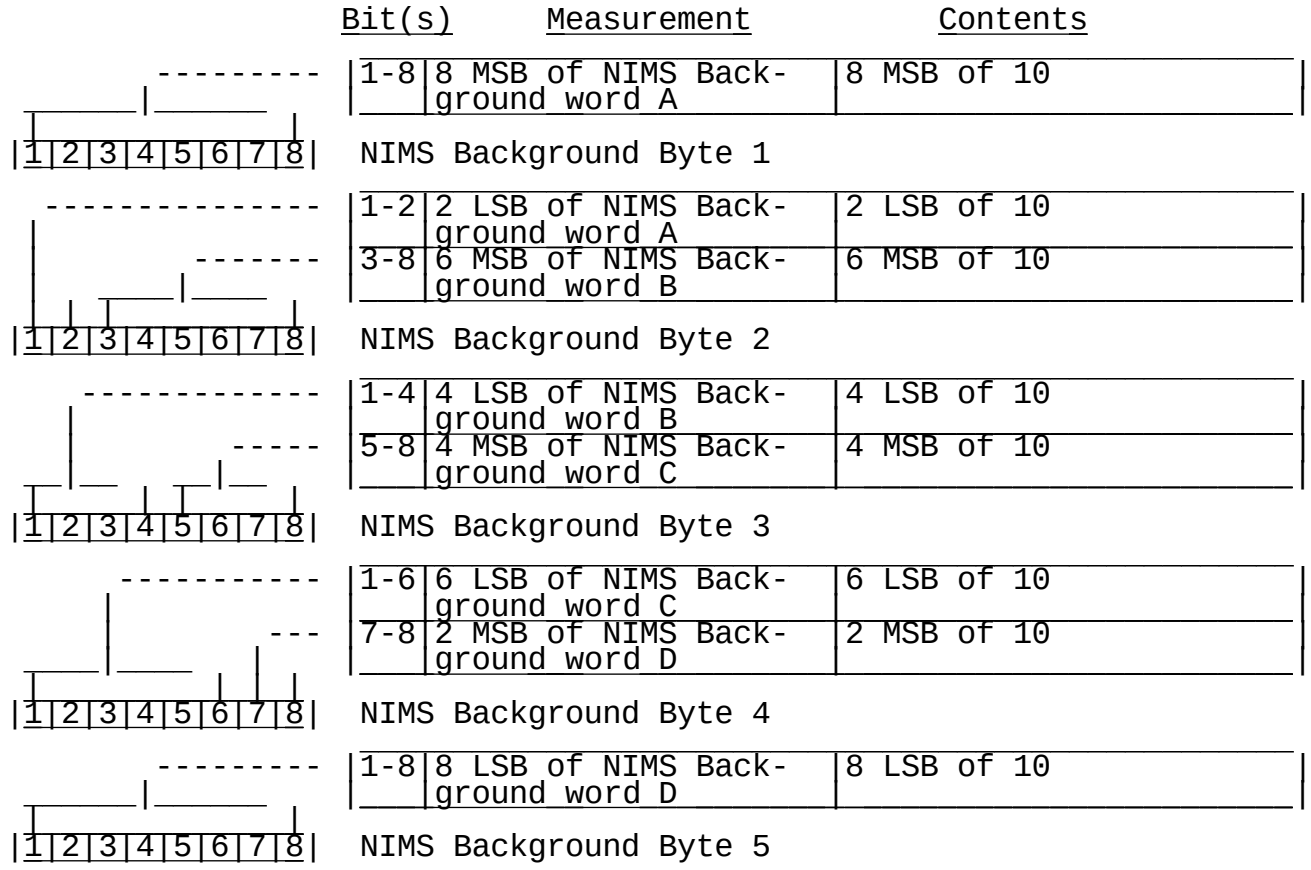
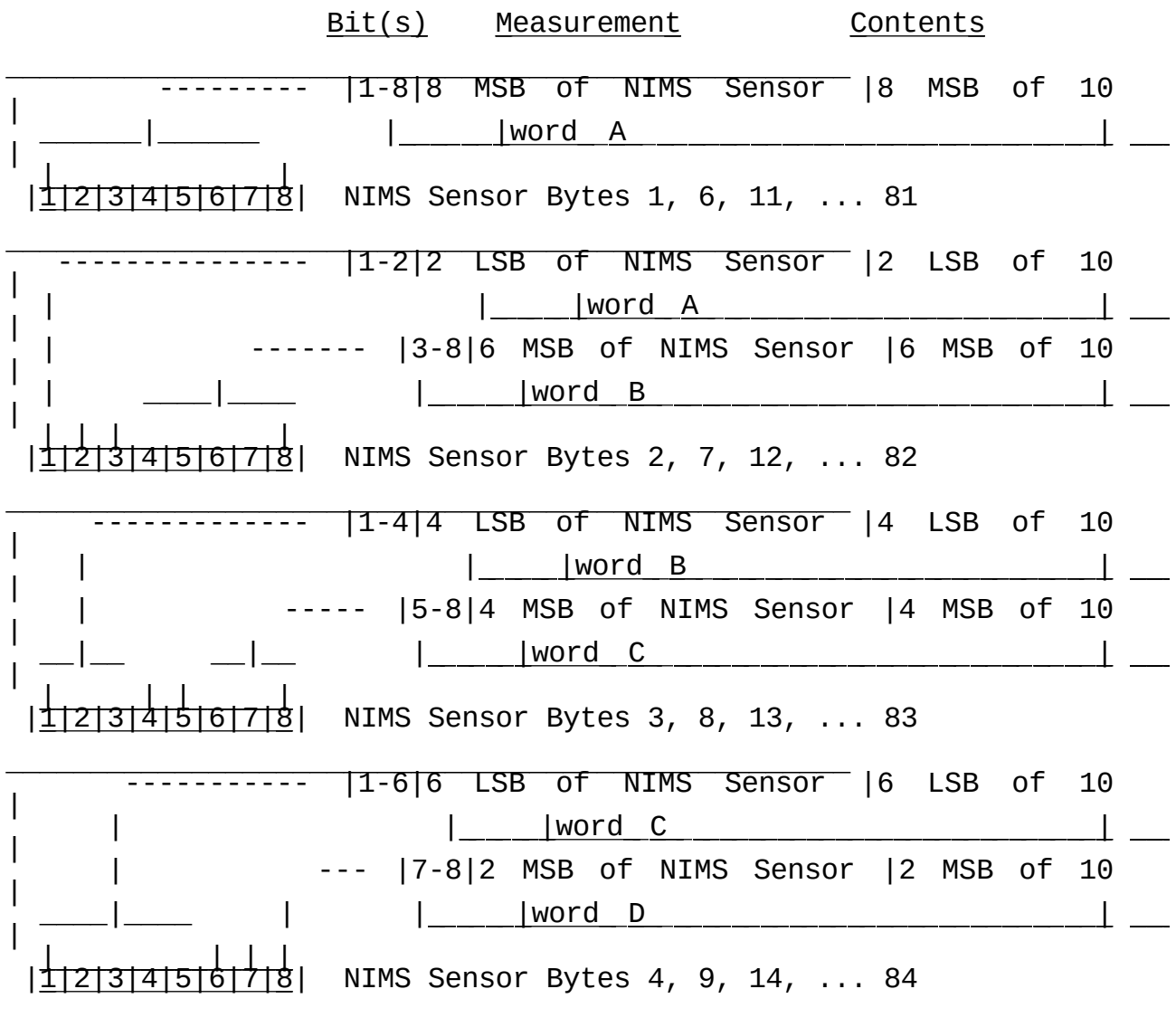


Table A2.8.6 NIMS Background Data Commutation

MOD 10 count	Word A	Word B	Word C	Word D
1, 6	detector 1	detector 2	detector 3	detector 4
2, 7	detector 5	detector 6	detector 7	detector 8
3, 8	detector 9	detector 10	detector 11	detector 12
4, 9	detector 13	detector 14	detector 15	detector 16
5, 0	detector 17	spare	spare	spare

A2.8.2.4 Sensor Data. The contents of the Sensor Data section is 85 bytes of infrared sensor data. Each block of 5 bytes contains 4 (10 bit) words of NIMS sensor data. This is shown in Table A2.8.7. Within each 5 MOD 10 counts, each of the 17 NIMS detectors are sampled 20 times. The commutation of this data into the packet is shown in Table A2.8.8. The chopper cycle of each sample is also given in Table A2.8.8, with N determined by Table A2.8.9.

Table A2.8.7 NIMS Sensor Data (MSB is bit 1)



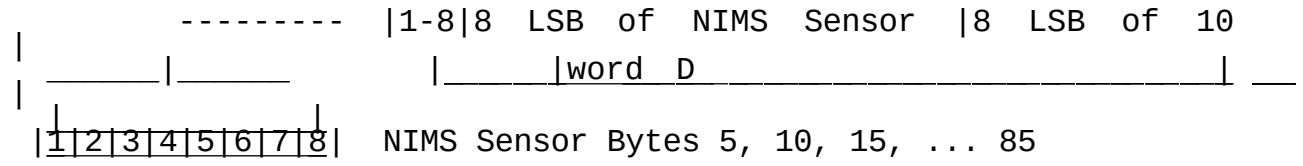

|1-8|8 LSB of NIMS Sensor |8 LSB of 10
|word D
|1|2|3|4|5|6|7|8|
NIMS Sensor Bytes 5, 10, 15, ... 85

Table A2.8.8 NIMS Sensor Data Commutation

	Word A		Word B		Word C		Word D	
Bytes	chopper cycle	sensor number	chopper cycle	sensor number	chopper cycle	sensor number	chopper cycle	sensor number
1-5	N	1	N	2	N	3	N	4
6-10	N	5	N	6	N	7	N	8
11-15	N	9	N	10	N	11	N	12
16-20	N	13	N	14	N	15	N	16
21-25	N	17	N+1	1	N+1	2	N+1	3
26-30	N+1	4	N+1	5	N+1	6	N+1	7
31-35	N+1	8	N+1	9	N+1	10	N+1	11
36-40	N+1	12	N+1	13	N+1	14	N+1	15
41-45	N+1	16	N+1	17	N+2	1	N+2	2
46-50	N+2	3	N+2	4	N+2	5	N+2	6
51-55	N+2	7	N+2	8	N+2	9	N+2	10
56-60	N+2	11	N+2	12	N+2	13	N+2	14
61-65	N+2	15	N+2	16	N+2	17	N+3	1
66-70	N+3	2	N+3	3	N+3	4	N+3	5
71-75	N+3	6	N+3	7	N+3	8	N+3	9
76-80	N+3	10	N+3	11	N+3	12	N+3	13
81-85	N+3	14	N+3	15	N+3	16	N+3	17

Table A2.8.9 NIMS Chopper Cycle Commutation

MOD 10 count	N
1, 6	0
2, 7	4
3, 8	8
4, 9	12
5, 0	16

A2.8.3 Telemetry Mode Changes. Upon the application of system power, NIMS shall automatically configure itself to an instrument safe mode. The Digital Status and Analog Engineering data shall be valid.

Commanded telemetry mode changes are processed just prior to every RIM change. Telemetry mode changes shall occur at the RIM change after command processing.

A2.9 PLASMA SUBSYSTEM TELEMETRY

This paragraph describes the format and content of the PLS output.

A2.9.1 PLS Packet. The schematic of the packet is shown in Figure A2.9.1. One full PLS packet is distributed over 364 LPW/LNR frames.

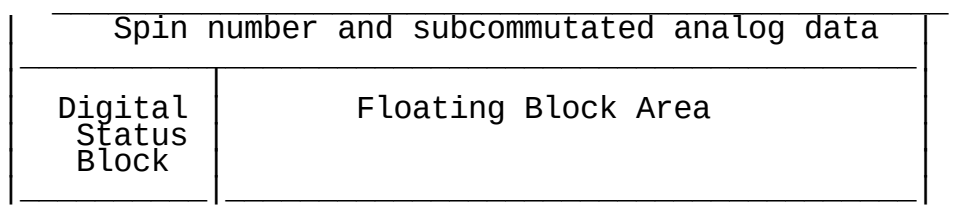


Figure A2.9.1 PLS Packet

A2.9.2 Instrument Synchronicity. Within the PLS packet, there will exist one major synchronism relative to the SCLK. The relationship between SCLK and PLS synchronization Index is shown in Table A2.9.1.

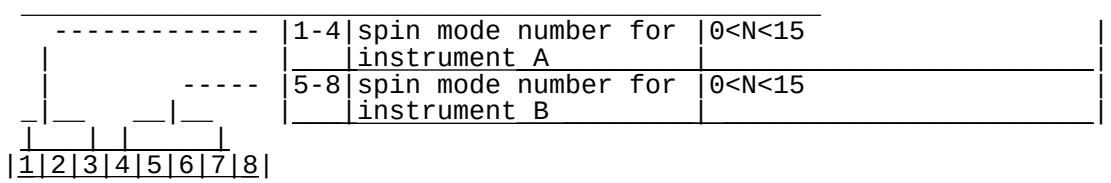
Table A2.9.1 SCLK vs. PLS S.I.

Rim (Modulo 4)	S.I.
0	Mod 91
1	91 + Mod 91
2	182 + Mod 91
3	273 + Mod 91

A2.9.3 PLS Fixed Telemetry. There are two areas of fixed telemetry in the PLS packet. The spin number and subcommutated Analog data are placed in the first two bytes of each PLS portion of an LPW/LNR frame. The Digital Status Block is located at the start of the PLS packet (S.I. equals 0).

A2.9.3.1 Spin Number and Subcommutated Analog Data. Bytes 1 and 2 of each PLS portion of an LPW/LNR frame contain the spin number pertaining to that frame, and subcommutated Analog data, respectively. The contents of the spin number byte are shown in Table A2.9.2.

Table A2.9.2 Spin Number



The subcommutated Analog Housekeeping is the second byte in all PLS portions of the LPW/LNR frame, and contains the data shown in Table A2.9.3. The relationship of these words to S.I. is also shown in Table A2.9.3.

Table A2.9.3. PLS Subcommutated Analog Housekeeping

Bits	Measurement	Content
1-8	detector bias monitor A	0 to 3800 volts

Byte 1, S.I. = 0, 1, 92, 183, 274

Bits	Measurement	Content
1-8	LVPS +27.0V A; plate/bias	0 to 40 volts

Byte 2, S.I. = 2, 93, 184, 275

Bits	Measurement	Content
1-8	LVPS +27.0V A; pull-down	0 to 40 volts

Byte 3, S.I. = 3, 94, 185, 276

Bits	Measurement	Content
1-8	LVPS +25.0V A	0 to 40 volts

Byte 4, S.I. = 4, 95, 186, 277

Bits	Measurement	Content
1-8	supplemental heater monitor	-35 to +50 deg. C

Byte 5, S.I. = 5, 96, 187, 278

Bits	Measurement	Content
1-8	LVPS +10.0V A	0 to 15 volts

Byte 6, S.I. = 6, 97, 188, 279

Bits	Measurement	Content
1-8	LVPS +7.5V A	0 to 10 volts

Byte 7, S.I. = 7, 98, 189, 280

Bits	Measurement	Content
1-8	LVPS +6.0V A	0 to 10 volts

Byte 8, S.I. = 8, 99, 190, 281

Table A2.9.3. PLS Subcommutated Analog Housekeeping

Bits	Measurement	Content
1-8	LVPS +5.0V A	0 to 10 volts

1|2|3|4|5|6|7|8 Byte 9, S.I. = 9, 100, 191, 282

Bits	Measurement	Content
1-8	LVPS -8.0V A	0 to -10 volts

1|2|3|4|5|6|7|8 Byte 10, S.I. = 10, 101, 192, 283

Bits	Measurement	Content
1-8	temperature regulator	-35 to 50 deg. C

1|2|3|4|5|6|7|8 Byte 11, S.I. = 11, 102, 193, 284

Bits	Measurement	Content
1-8	7.8V T monitor (open) temperature; m.s. 2 housing (closed)	0 to 127=cover open, voltage monitor 128 to 255=cover closed, temperature -35 to 50 deg. C

1|2|3|4|5|6|7|8 Byte 12, S.I. = 12, 103, 194, 285

Bits	Measurement	Content
1-8	7.8V T monitor (closed) temperature; m.s. 2 housing (open)	0 to 127=cover closed, voltage monitor 128 to 255=cover open, temperature -35 to 50 deg. C

1|2|3|4|5|6|7|8 Byte 13, S.I. = 13, 104, 195, 286

Bits	Measurement	Content
1-8	analog ground reference A	0.0 volts

1|2|3|4|5|6|7|8 Byte 14, S.I. = 14, 105, 196, 287

Bits	Measurement	Content
1-8	detector bias monitor B	0 to 3800 volts

1|2|3|4|5|6|7|8 Byte 15, S.I. = 15, 106, 197, 288

Bits	Measurement	Content
1-8	LVPS +27.0V B; plate/ bias	0 to 40 volts

1|2|3|4|5|6|7|8 Byte 16, S.I. = 16, 107, 198, 289

Table A2.9.3. PLS Subcommutated Analog Housekeeping

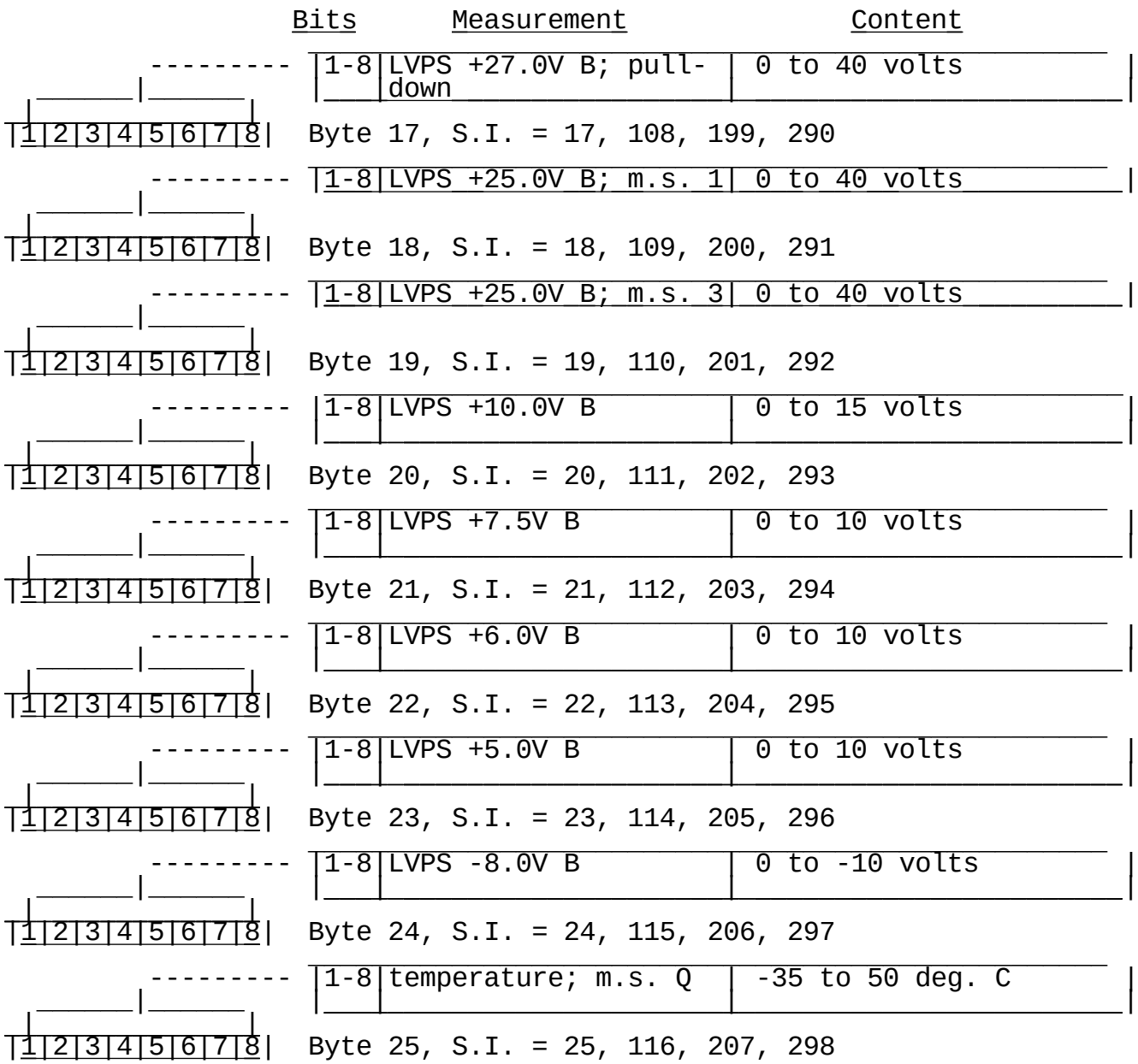


Table A2.9.3. PLS Subcommutated Analog Housekeeping

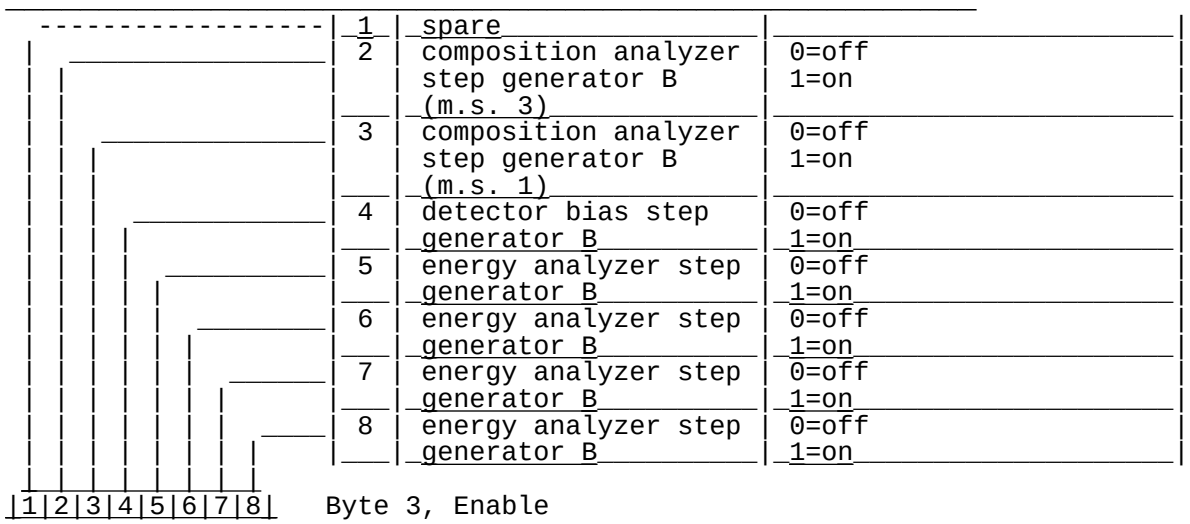
Bits	Measurement	Content
1-8	temperature; bias A	-35 to 50 deg. C
1|2|3|4|5|6|7|8	Byte 26, S.I. = 26, 117, 208, 299	
1-8	Analog ground reference B	0.0 volts
1|2|3|4|5|6|7|8	Byte 27, S.I. = 27, 118, 209, 300	
1-8	energy analyzer A HV monitor steps 0 to 63	0 to 2600 volts
1|2|3|4|5|6|7|8	Byte 28 to 91, S.I. = 28 - 91	
1-8	energy analyzer B HV monitor steps 0 to 63	0 to 2600 volts
1|2|3|4|5|6|7|8	Byte 92 to 155, S.I. = 119 - 182	
1-8	composition analyzer current monitor A steps 0 to 63	0 to 300 ma
1|2|3|4|5|6|7|8	Byte 156 to 219, S.I. = 210 - 273	
1-8	composition analyzer current monitor B steps 0 to 63	0 to 300 ma
1|2|3|4|5|6|7|8	Byte 220 to 283, S.I. = 301 - 364	

A2.9.3.2 Digital Status Block. The Digital Status Block is located at the start of the PLS packet (S.I. equals 0). The contents of this block are shown in Figure A2.9.2., and the bit definitions of the digital status bytes are shown in Table A2.9.4.

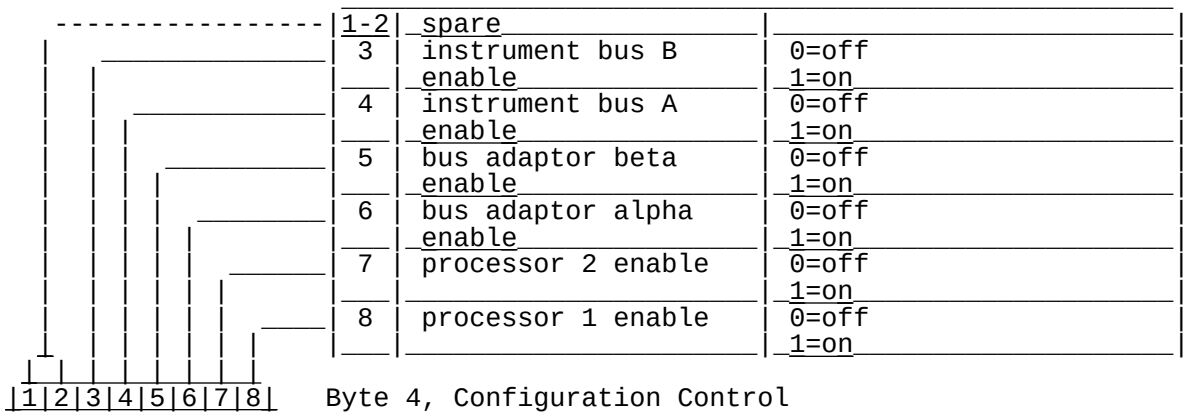
Byte 1	Block I. D. (06)
Byte 2	Block Size (47)
Byte 3	Enable Byte
Byte 4	Configuration Control Byte
Byte 5	Power Switching Byte
Byte 6	AACS S/C Clock Sectoring Byte
/ \ /	/ \ /
Byte 49	Last Critical Telemetry Byte

Figure A2.9.2. Digital Status Block

Table A2.9.4. Digital Status Data

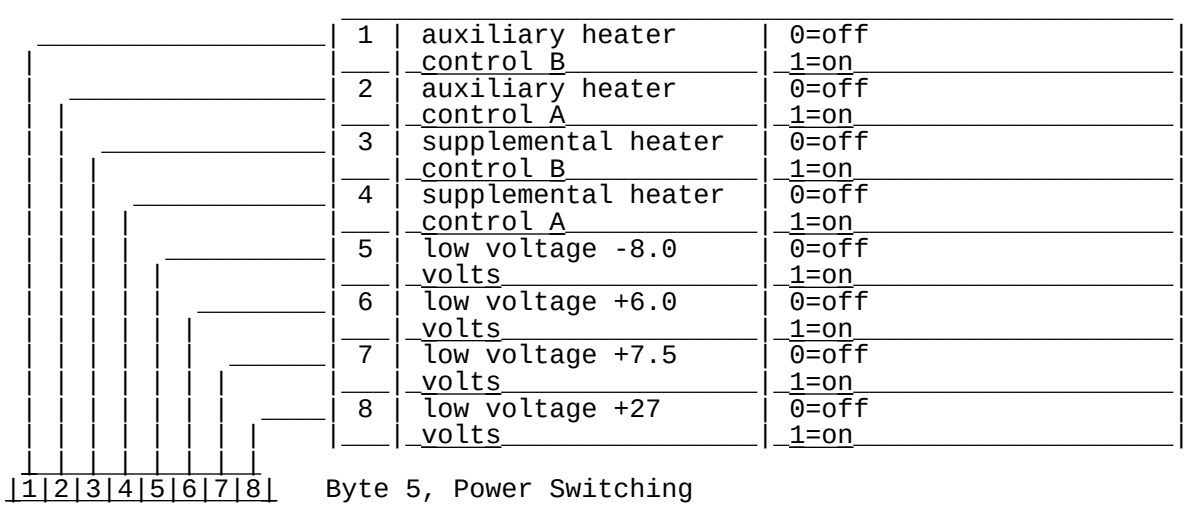


Byte 3, Enable

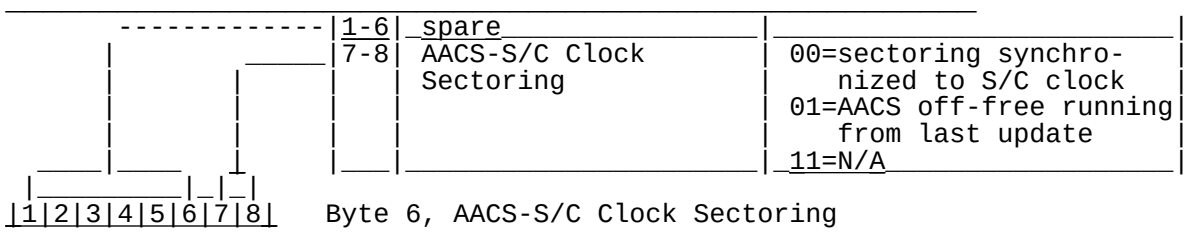


Byte 4, Configuration Control

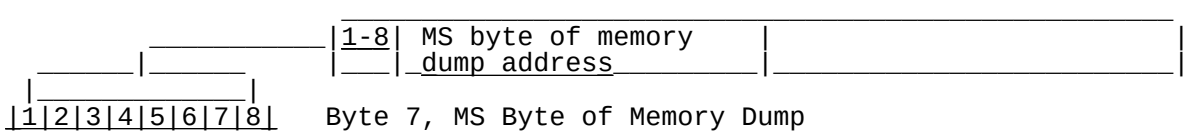
Table A2.9.4. Digital Status Data



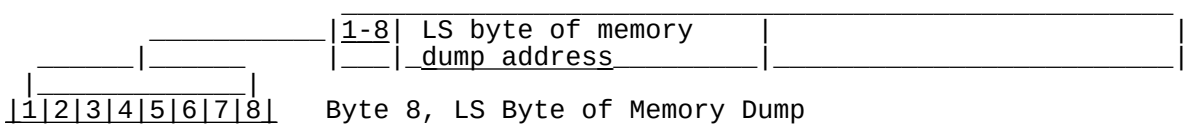
Byte 5, Power Switching



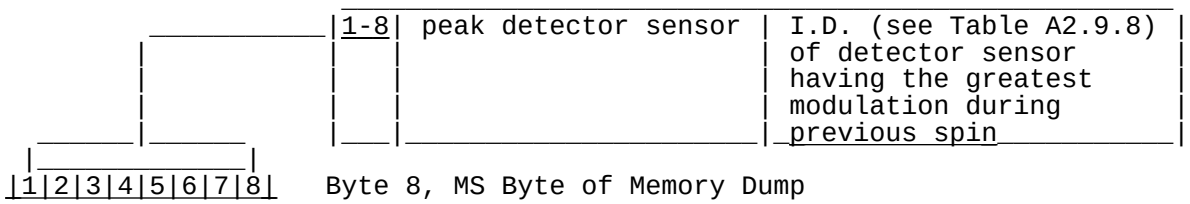
Byte 6, AACS-S/C Clock Sectoring



Byte 7, MS Byte of Memory Dump

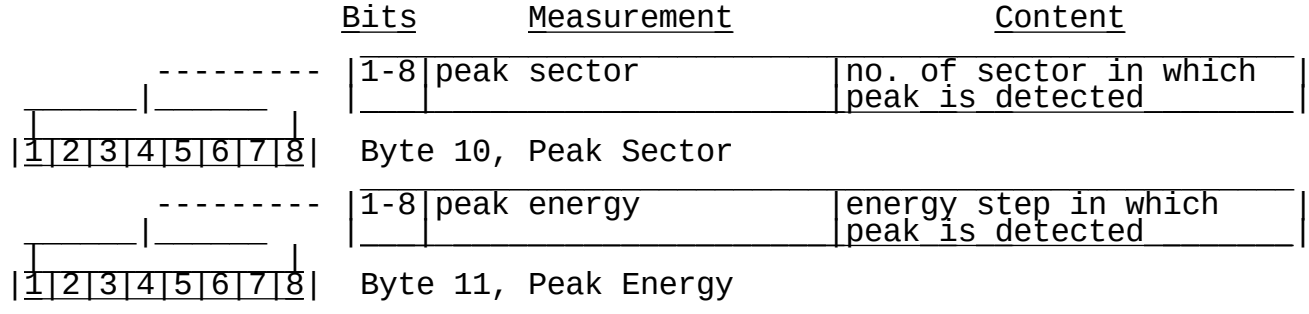


Byte 8, LS Byte of Memory Dump



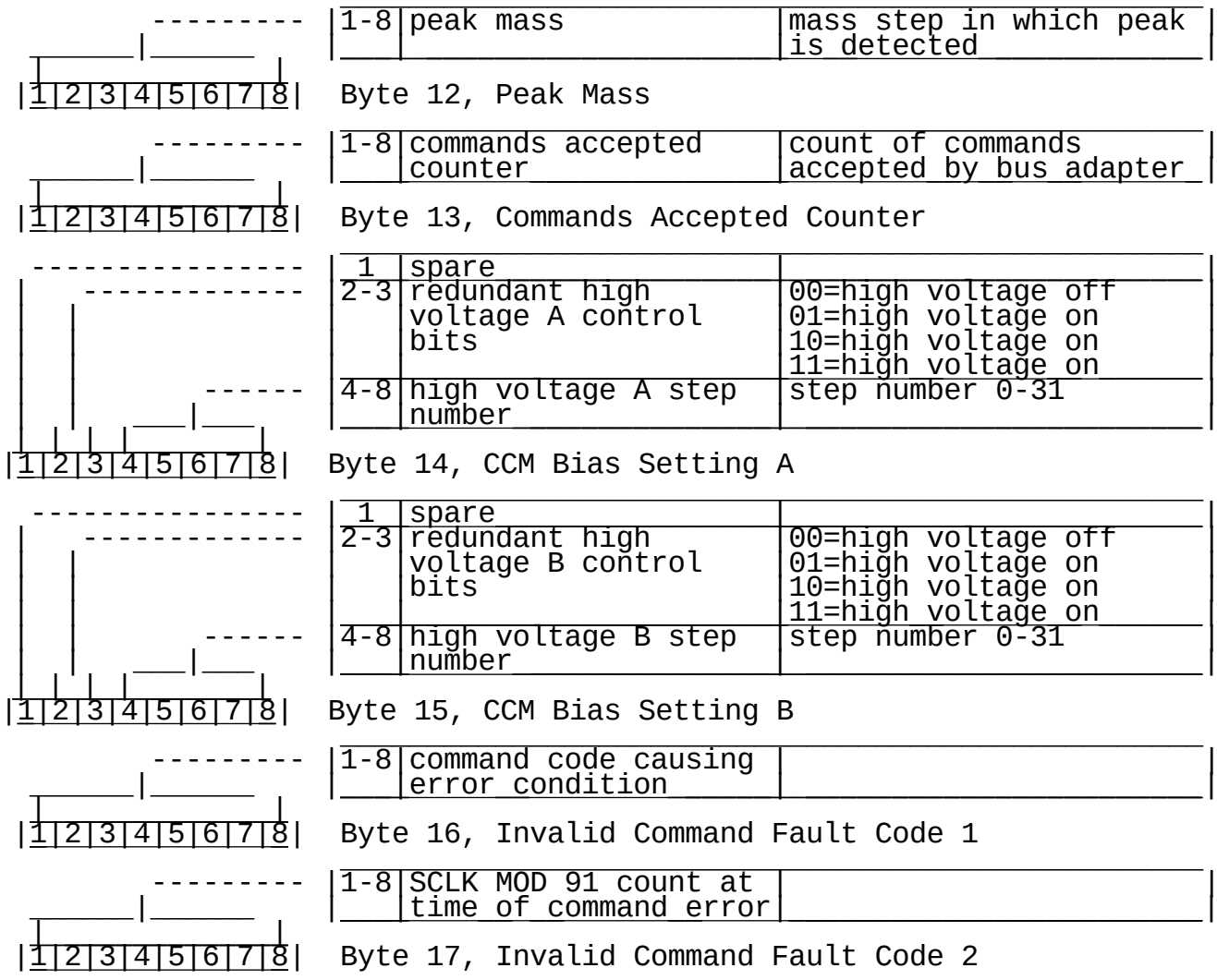
Byte 8, MS Byte of Memory Dump

Table A2.9.4. Digital Status Data



Byte 10, Peak Sector

Byte 11, Peak Energy



1-8	peak mass	mass step in which peak is detected	

1|2|3|4|5|6|7|8 Byte 12, Peak Mass

1-8	commands accepted counter	count of commands accepted by bus adapter	

1|2|3|4|5|6|7|8 Byte 13, Commands Accepted Counter

1	spare		
2-3	redundant high voltage A control bits	00=high voltage off 01=high voltage on 10=high voltage on 11=high voltage on	
4-8	high voltage A step number	step number 0-31	

1|2|3|4|5|6|7|8 Byte 14, CCM Bias Setting A

1	spare		
2-3	redundant high voltage B control bits	00=high voltage off 01=high voltage on 10=high voltage on 11=high voltage on	
4-8	high voltage B step number	step number 0-31	

1|2|3|4|5|6|7|8 Byte 15, CCM Bias Setting B

1-8	command code causing error condition		

1|2|3|4|5|6|7|8 Byte 16, Invalid Command Fault Code 1

1-8	SCLK MOD 91 count at time of command error		

1|2|3|4|5|6|7|8 Byte 17, Invalid Command Fault Code 2

Table A2.9.4. Digital Status Data

Bits	Measurement	Content
1-4	LSB's of SCLK Real-time image count at time of command error	
5-8	SCLK MOD 10 count at time of command error	

|1|2|3|4|5|6|7|8|

Byte 18, Invalid Command Fault Code 3

Bits	Measurement	Content
1-8	invalid command count during PLS instrument cycle	

|1|2|3|4|5|6|7|8|

Byte 19, Invalid Command Fault Code 4

Bits	Measurement	Content
1-8	SCLK MOD 91 count at time of heater fault	

|1|2|3|4|5|6|7|8|

Byte 20, Supplemental Heater Monitor Fault Code 1

Bits	Measurement	Content
1-4	LSB's of SCLK Real-time image count at time of heater fault	
5-8	SCLK MOD 10 count at time of heater fault	

|1|2|3|4|5|6|7|8|

Byte 21, Supplemental Heater Monitor Fault Code 2

Bits	Measurement	Content
1-8	heater fault count during PLS instrument cycle	

|1|2|3|4|5|6|7|8|

Byte 22, Supplemental Heater Monitor Fault Code 3

Bits	Measurement	Content
1-4	spare	
5	ROM address 0C00 to 0FFF (HEX)	0=no error detected 1=error detected
6	ROM address 0800 to 0BFF (HEX)	0=no error detected 1=error detected
7	ROM address 0400 to 07FF (HEX)	0=no error detected 1=error detected
8	ROM address 0000 to 03FF (HEX)	0=no error detected 1=error detected

|1|2|3|4|5|6|7|8|

Byte 23, Memory Fault Code 1

Table A2.9.4. Digital Status Data

Bits	Measurement	Content
1	RAM address 1700 to 17FF (HEX)	0=no error detected 1=error detected
2	RAM address 1600 to 16FF (HEX)	0=no error detected 1=error detected
3	RAM address 1500 to 15FF (HEX)	0=no error detected 1=error detected
4	RAM address 1400 to 14FF (HEX)	0=no error detected 1=error detected
5	RAM address 1300 to 13FF (HEX)	0=no error detected 1=error detected
6	RAM address 1200 to 12FF (HEX)	0=no error detected 1=error detected
7	RAM address 1100 to 11FF (HEX)	0=no error detected 1=error detected
8	RAM address 1000 to 10FF (HEX)	0=no error detected 1=error detected

|1|2|3|4|5|6|7|8| Byte 24, Memory Fault Code 2

Bits	Measurement	Content
1	RAM address 1F00 to 1FFF (HEX)	0=no error detected 1=error detected
2	RAM address 1E00 to 1EFF (HEX)	0=no error detected 1=error detected
3	RAM address 1D00 to 1DFF (HEX)	0=no error detected 1=error detected
4	RAM address 1C00 to 1CFF (HEX)	0=no error detected 1=error detected
5	RAM address 1B00 to 1BFF (HEX)	0=no error detected 1=error detected
6	RAM address 1A00 to 1AFF (HEX)	0=no error detected 1=error detected
7	RAM address 1900 to 19FF (HEX)	0=no error detected 1=error detected
8	RAM address 1800 to 18FF (HEX)	0=no error detected 1=error detected

|1|2|3|4|5|6|7|8| Byte 25, Memory Fault Code 3

1-8	spare	

|1|2|3|4|5|6|7|8| Byte 26-38, spares

1-8	CDS bus parity error count (H/W)	

|1|2|3|4|5|6|7|8| Byte 39, CDS Bus Parity Error

Table A2.9.4. Digital Status Data

Bits	Mesurement	Content
1-8	PLS bus parity error count (S/W)	

|1|2|3|4|5|6|7|8|

Byte 40, PLS Bus Parity Error

Bits	Mesurement	Content
1-8	A accumulator over-flow error count	

|1|2|3|4|5|6|7|8|

Byte 41, A Accumulator Overflow Error

Bits	Mesurement	Content
1-8	A accumulator over-flow spinmode sequence number	

|1|2|3|4|5|6|7|8|

Byte 42, A Accumulator Overflow Spinmode

Bits	Mesurement	Content
1-8	B accumulator over-flow error count	

|1|2|3|4|5|6|7|8|

Byte 43, B Accumulator Overflow Error

Bits	Mesurement	Content
1-8	B accumulator over-flow spinmode sequence number	

|1|2|3|4|5|6|7|8|

Byte 44, B Accumulator Overflow Spinmode

Bits	Mesurement	Content
1-8	critical telemetry buffer	TBD

|1|2|3|4|5|6|7|8|

Byte 45-49, Critical Telemetry Buffer

A2.9.4 Floating Block Area. The Floating Block area is divided into 12 spin areas. The boundaries between spin areas are not fixed, but vary based on the size and number of blocks contained.

All blocks start with a one byte block ID code which specifies the type of block. All blocks then contain a one byte block length (except for sensor data blocks, para. A2.9.4.6.), followed by block entries. Some blocks always end with a one byte end code (FF_{hex}).

If a given block of this type cannot be completed within a given LPW/LNR frame, floating blocks in subsequent frames will have the same block I.D. code and the block will continue until a block with that code terminates in (FF_{hex}).

The first spin area, in all PLS packets, will contain all blocks required to identify and process the science data contained in spin area 1. Subsequently , only changes or additions to the blocks will be contained within the spin area.

Blocks which can appear in the spin areas are shown in Table A2.9.5, in the order in which they occur. Not all blocks must appear in each spin. Additional blocks, which can occur anywhere in the floating block area, are shown in Table A2.9.6.

Table A2.9.5. Ordered Blocks

Block ID code		Length (bytes)	Para.
30	Mode Sequencing Block A	13	A2.9.4.1
32	Mode Sequencing Block B	13	A2.9.4.1
20	Sensor Sequencing Block A	N* (11 max.)	A2.9.4.2
22	Sensor Sequencing Block B	N (11 max.)	A2.9.4.2
28	Sector Sequencing Block A	6	A2.9.4.3
2A	Sector Sequencing Block B	6	A2.9.4.3
24	High Voltage Sequencing Block A	4	A2.9.4.4
26	High Voltage Sequencing Block B	4	A2.9.4.4
2C	Mass Analyzer Sequencing Block A	N (65 max.)	A2.9.4.5
2E	Mass Analyzer Sequencing Block B	N (65 max.)	A2.9.4.5
40+block count	Sensor Data A	N (1280 max)	A2.9.4.6
40+block count	Sensor Data B	N (1280 max)	A2.9.4.6

* size varies

Table A2.9.6. Non-ordered Blocks

Block ID code		Length (bytes)	Para.
00	NOP (fill)	N (47 max.)	A2.9.4.7
04	Analog Housekeeping	N (47 max.)	A2.9.4.10
06	Digital Status*	47	A2.9.3.2
08	Analog Sequencing Block	N (47 max.)	A2.9.4.9

* Occurs at start of every PLS packet.

A2.9.4.1 Mode Sequencing Block. The Mode Sequencing Block consists of 15 bytes of data, 12 of which determine the mode which the instrument is in for the 12 respective spins. The constents are shown in Figure A2.9.3, with the modes shown in Table A2.9.7.

Byte 1	Block I. D.
Byte 2	Block Size (13)
Byte 3	Mode number of spin 1 (see Table A2.9.9 for mode types
Byte 4	Mode number of spin 2 (see Table A2.9.9 for mode types
Byte 5	Mode number of spin 3 (see Table A2.9.9 for mode types
Byte 6	Mode number of spin 4 (see Table A2.9.9 for mode types
Byte 7	Mode number of spin 5 (see Table A2.9.9 for mode types
Byte 8	Mode number of spin 6 (see Table A2.9.9 for mode types
Byte 9	Mode number of spin 7 (see Table A2.9.9 for mode types
Byte 10	Mode number of spin 8 (see Table A2.9.9 for mode types
Byte 11	Mode number of spin 9 (see Table A2.9.9 for mode types
Byte 12	Mode number of spin 10 (see Table A2.9.9 for mode types
Byte 13	Mode number of spin 11 (see Table A2.9.9 for mode types
Byte 14	Mode number of spin 12 (see Table A2.9.9 for mode types
Byte 15	End Code (FF HEX)

Figure A2.9.3. Mode Sequencing Blocks

Table A2.9.7. PLS Modes

Mode Number	PLS Instrument A Mode	PLS Instrument B Mode
1	Velocity Distribution Survey	Velocity Distribution Survey
2	Beam Velocity Distribution	Beam Velocity Distribution
3	Mass Composition Survey (Detectors 2MI, 2MD)	Mass Composition Survey (Detectors 1MI, 1MD)
4	N/A	Mass Composition Survey (Detectors 3MI, 3MD)
5	Beam Mass Composition	Beam Mass Composition

A2.9.4.2 Sensor Sequencing Block. The Sensor Sequencing Block consists of an arbitrary number of detector I. D. words, terminated by a byte containing an End Code (FF_{HEX}).

Figure A2.9.4. depicts the contents of this block, and Table A2.9.8. shows the sensor I. D.'s.

Byte 1	Block I. D. (20=A, 22=B, HEX)
Byte 2	Block Size (N)
Byte 3	First sensor I. D.
Byte 4	Second sensor I. D.
Byte 5	Third sensor I. D.
Byte 6	Fourth sensor I. D.
/	/ /
\	\ \
/	/ /
Byte N+1	Last sensor I. D.
Byte N+2	End Code (FF HEX)

Figure A2.9.4. PLS Sensor Sequencing Block

Table A2.9.8. PLS Sensor I. D. Codes

I. D. Code	Sensor
02	2MI
06	1P
0A	3P
0E	5P
12	7P
42	2MD
46	1E
4A	3E
4E	5E
52	7E
82	1MI
86	3MI
8A	2P
8E	4P
92	6P
C2	1MD
C6	3MD
CA	2E
CE	4E
D2	6E

A2.9.4.3 Sector Sequencing Block. The Sector Sequencing Block consists of 8 bytes of data. Five of those determine the sector sequencing for the spin it is in, and subsequent spins until it is updated, or a new PLS packet starts. The contents of this block are shown in Figure A2.9.5.

Byte 1	Block I.D. (28=A, 2A=B, HEX)
Byte 2	Block Size (6)
Byte 3	AACS Clock angle of start of first sector (0 to 360 degrees, see A2.4, AACS Position and Rate Date)
Byte 4	Duration of each energy (or mass) step, in 8.33 ms units
Byte 5	Number of steps to be scanned in this sector
Byte 6	Clock angle increment to start of next sector
Byte 7	Number of sectors to be sampled in one spin
Byte 8	End Code (FF HEX)

Figure A2.9.5. Sector Sequencing Blocks

A2.9.4.4 High Voltage Sequencing Block. The High Voltage Sequencing Block contains 6 bytes, 3 of which determine the high voltage sequence gone through. The contents of this block are shown in Figure A2.9.6.

Byte 1	Block I.D. (24=A, 26=B, HEX)
Byte 2	Block Size (4)
Byte 3	Initial Step Number
Byte 4	Step Number Increment
Byte 5	Final Step Number
Byte 6	End Code (FF HEX)

Figure A2.9.6 High Voltage Sequencing Blocks

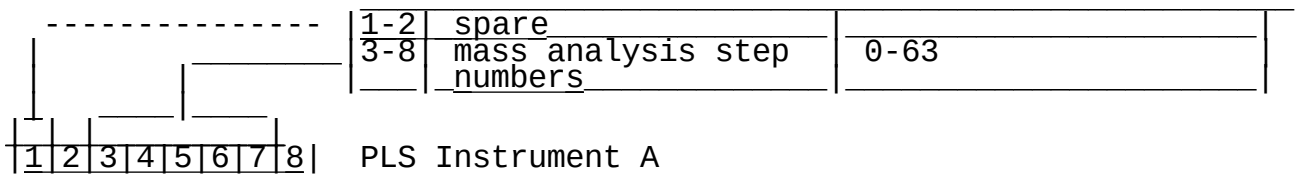
A2.9.4.5 Mass Analyzer Sequencing Block. The Mass Analyzer Sequencing Block contains lists of mass analyzer step numbers. The list is terminated by an entry of FF. hex

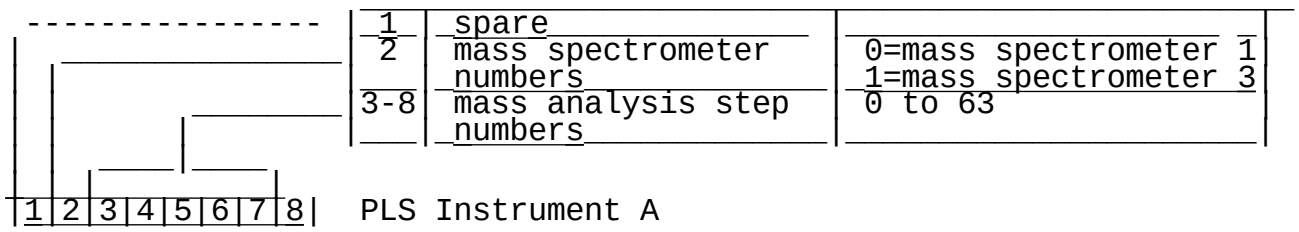
This block is shown in Figure A2.9.7. The bit definitions of the step number bytes is shown in Table A2.9.9.

Byte 1	Block I.D. (2C=A, 2E=B, HEX)
Byte 2	Block Size (N)
Byte 3	First mass analysis step number
Byte 4	Second mass analysis step number
Byte 5	Third mass analysis step number
Byte 6	Fourth mass analysis step number
/ \ /	/ \ /
Byte N+1	Last mass analysis step number
Byte N+2	End Code (FF HEX)

Figure A2.9.7. Mass Analyzer Sequencing Blocks

Table A2.9.9. Mass Analysis step number bit definitions





A2.9.4.6 Sensor Data Block. The Sensor Data Block contains sensor data, arranged in a sequence determined by the previously mentioned Sequencing Blocks. The sequence begins with the first sensor listed in the latest avaliable Sensor Sequencing Block, at the first entry in the latest Mass Analyzer Sequencing block, at the first entry in the latest High Voltage Sequencing block, and at the first entry in the latest Sector Sequencing block. After going through all entries in the Sensor Sequencing Block, it goes to the next entry in the Mass Analyzer Sequencing Block, then goes through the Sensor Sequencing Block again. This process is illustrated in Figure A2.9.8. This block is shown in Figure A2.9.9 The sensor data itself is logarithmically compressed. The decompression algorithm is given in Figure A2.9.10.

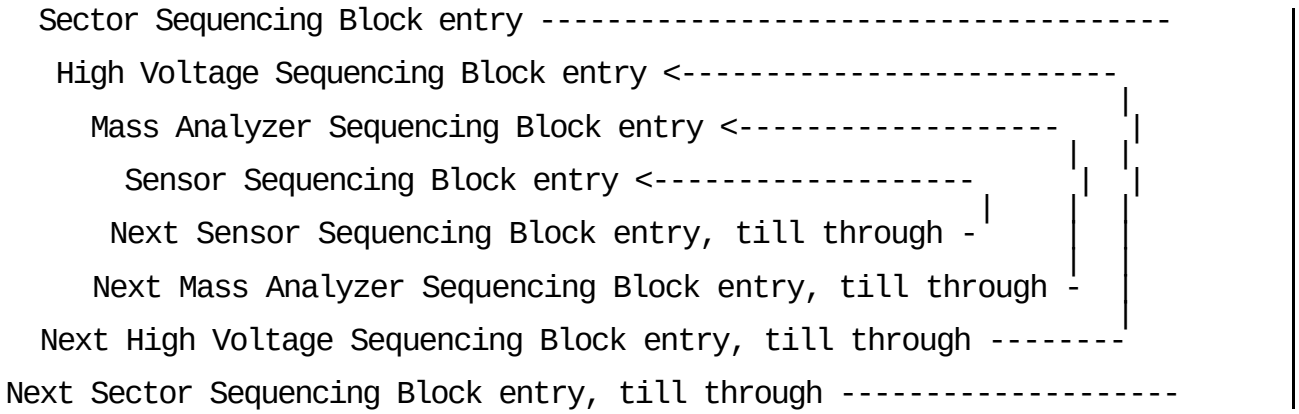


Figure A2.9.8. Sequencing of Sensor Data Block Entries.

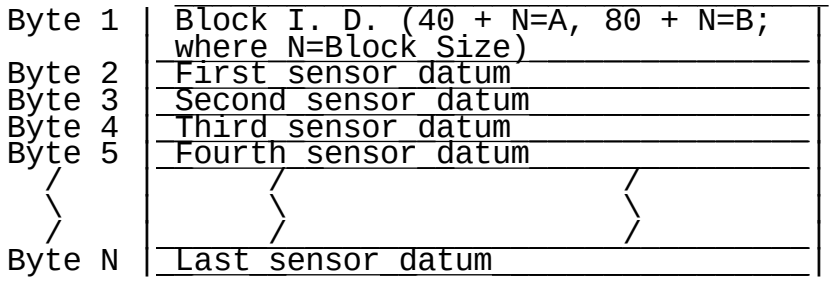
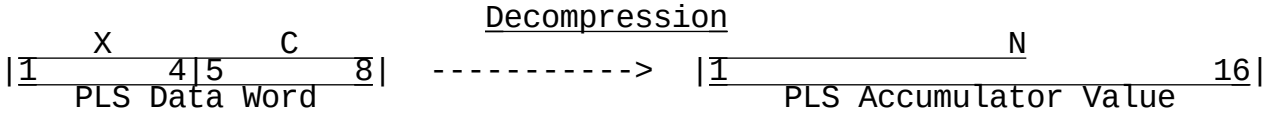


Figure A2.9.9. Sensor Data Blocks



Algorithm: for X=0 N=C

for X>0 $N=(16+C)\,2^{(X-1)}$

.

Figure A2.9.10. Sensor Data Decompression Algorithm

A2.9.4.7 NOP (Fill) Block. The NOP block contains fill data used to fill the PLS telemetry allocation when no useful data is availiable. The contents of this block is shown in Figure A2.9.11.

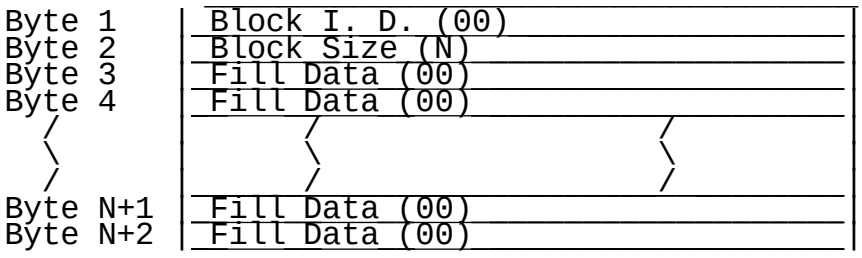


Figure A2.9.11. NOP Block

A2.9.4.8 Deleted.

Figure A2.9.12. Deleted

A2.9.4.9 Analog Sequencing Block. This block specifies the contents of the Analog Housekeeping Block. The contents are shown in Figure A2.9.13. The measurements corresponding to the allowable values are shown in Table A2.9.10.

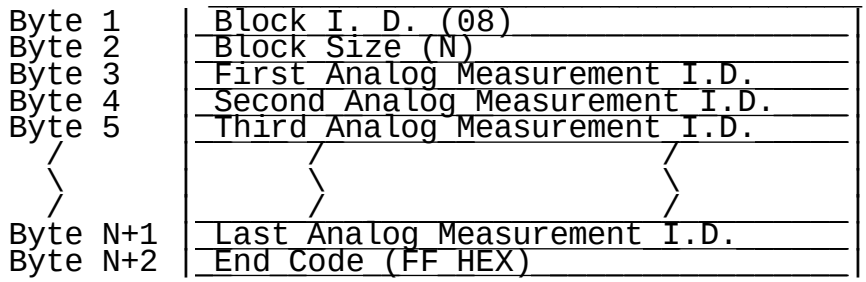


Figure A2.9.13. Analog Sequencing Block

Table A2.9.10. PLS Analog Measurement I. D. Codes

I.D. Code	Instrument	Measurement	Contents
00	A	energy analyzer high voltage	0 to 2600 volts
01	A	detector bias high voltage	0 to 3800 volts
02	A	composition analyzer current	0 to 150 ma
03	A	LVPS current	0 to 200 ma
04	A	energy analyzer current	0 to 20 ma
05	A	LVPS -8.0 volts	0 to -10 volts
06	A	LVPS +5 volts	0 to 8 volts
07	A	LVPS +6.5 volts	0 to 8 volts
08	A	LVPS +7.5 volts	0 to 10 volts
09	A	LVPS +10 volts	0 to 15 volts
0A	A	LVPS +27 volts	0 to 40 volts
0B	A	0 volts ref./ cover deploy	0 to 5 volts 0 volts=deployed 3 volts=closed
0C	A	temperature transducer	-78 to 100 degrees
0D	A	detector bias current	0 to 30 ma
0E	A	supplemental heater control	0 to 5 volts
0F	A	spare	
10	B	energy analyzer high voltage	0 to 2600 volts
11	B	detector bias high voltage	0 to 3800 volts

Table A2.9.10. PLS Analog Measurement I. D. Codes

I.D. Code	Instrument	Measurement	Contents
12	B	composition analyzer current	0 to 150 ma
13	B	LVPS current	0 to 200 ma
14	B	energy analyzer current	0 to 20 ma
15	B	LVPS -8.0 volts	0 to -10 volts
16	B	LVPS +5 volts	0 to 8 volts
17	B	LVPS +6.5 volts	0 to 8 volts
18	B	LVPS +7.5 volts	0 to 10 volts
19	B	LVPS +10 volts	0 to 15 volts
1A	B	LVPS +27 volts	0 to 40 volts
1B	B	0 volts ref./ cover deploy	0 to 5 volts 0 volts=deployed 3 volts=closed
1C	B	temperature transducer	-78 to 100 degrees
1D	B	detector bias current	0 to 30 ma
1E	B	spare	
1F	B	spare	

A2.9.4.10 Analog Housekeeping Block. This block is in addition to the fixed Subcommutated Analog Housekeeping. This block contains analog data whose contents are specified by the Analog Sequencing Block, para. A2.9.4.3. The contents are shown in Figure A2.9.14

Byte 1	Block I. D. (04)
Byte 2	Block Size (N)
Byte 3	First Analog Measurement Value
Byte 4	Second Analog Measurement Value
Byte 5	Third Analog Measurement Value
Byte 6	Fourth Analog Measurement Value
/	/ /
\	\ \
/	/ /
Byte N+1	Last Analog Measurement Value
Byte N+2	End Code (FF HEX)

Figure A2.9.14. Analog Housekeeping Block

A2.9.5 Telemetry Mode Changes. Upon the application of system power, PLS shall disable its high voltage, and configure itself to the instrument synchronicity shown in Table A2.9.1, and at the beginning of the next cycle, generate valid telemetry. Commanded telemetry mode changes shall be processed at the time of receipt. Telemetry mode changes shall occur at the beginning of the instrument cycle.

A2.10 PHOTOPOLARIMETER RADIOMETER SUBSYSTEM TELEMETRY

These paragraphs describe the format and content of the PPR output.

A2.10.1 PPR Packet. The schematic of a PPR packet is shown in Figure A2.10.1. One PPR packet is placed in each LPW, LNR and LPU TDM telemetry frame. Fourteen PPR packets are contained in BPT TDM telemetry frames.

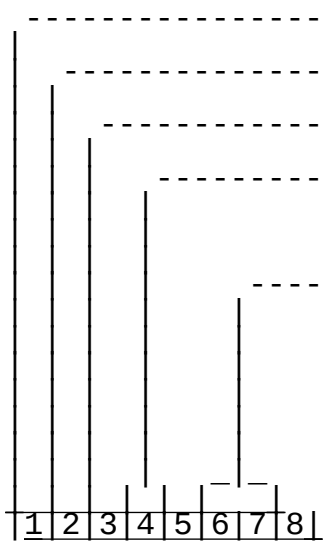
Title	Instrument Status	Status & Science	PPR Sci. Data 1	PPR Sci. Data 2	PPR Sci. Data 3
Data Offset	0	48	56	80	112
Bits/packet	48	8	24	32	32
Description	A2.10.3	A2.10.4	A2.10.5	A2.10.6	A2.10.7

Figure A2.10.1 PPR Packet

A2.10.2 Instrument Synchronicity. The contents of the PPR packet are uniquely determined by data available within the packet.

A2.10.3 Instrument Status. The contents of the digital status section are shown in Table A2.10.1.

Table A2.10.1 PPR Instrument Status (MSB is bit 1)

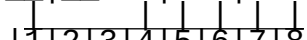


PPR Byte #1

Bit(s)	Measurement	Contents
1	memory ID	0=memory #1 1=memory #2
2	command parity	0=no parity error 1=parity error
3	telemetry/sector parity	0=no parity error 1=parity error
4-5	valid command count (MOD 4)	00=command #0 01=command #1 10=command #2 11=command #3
6-8	mode	000=transition 001=cycle 1 010=PP/Ph 011=Ph 100=Rad 101=Position Select 110=Cycle 6 111=Cycle 7

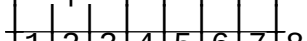
Table A2.10.1 PPR Instrument Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1-4	Gain PP/Ph	Gain Step 0-15
5-6	Gain Rad	Gain Step 0-3
7-8	Number of samples	00=1 sample 01=4 samples 10=16 samples 11=256 samples



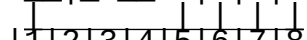
PPR Byte #2

1	number of samples multiplier	0=x1 1=x4
2-3	number of positions	00=0 00=1 10=2 11=5
4	calibration lamp	0=off 1=on
5	DCR initiate	0=inhibit 1=enable
6	boom sequence operation	0=inhibit 1=enable
7	chopper heater	0 (inoperative)
8	telemetry sent	0=current memory not read out 1=current memory read out



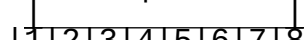
PPR Byte #3

1-5	programmed Filter/ Retarder position	position 0-31
6	temperature range	0=low 1=high
7	spare	
8	hskp status parity	set to yield odd parity in bytes 1-6



PPR Byte #4

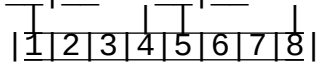
1-8	temperature data MSBs	8 MSBs of temp data (12 bits total)



PPR Byte #5

Table A2.10.1 PPR Instrument Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1-4	temperature data LSBs	4 L.S.Bs of temp data (12 bits total)
5-8	temperature ID	0000=RCT-1 0001=RCT-R 0010=RCT-2 0011=PRM-1 0100=PRM-2 0101=SEM-1 0110=CHM-2 0111=RAS-1A 1000=RAS-1B 1001=RAS-2A 1010=RAS-2B 1011=BRREF 1100=SCBAF 1101=N/A 1110=N/A 1111=N/A

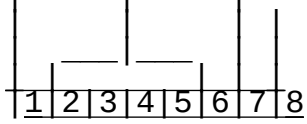


PPR Byte #6

A2.10.4 Status and Science. The status and science section of the packet contains information used both for determining the health of the instrument, and for science purposes. The contents are shown in Table A2.10.2.

Table A2.10.2 Status and Science (MSB is bit 1)

Bit(s)	Measurement	Contents
1	rad data #1	for samples #1A and 1B 0=PP/PH scene science data 1=rad scene science data & science temperature
2-6	Filter/Retarder position #1	identifies the FRP position (0-31) corresponding to scene samples of bytes 8-10 (bit 2 is MSB)
7	calibration/boom tag #1	0=last sample pair taken during S/C roll with boom sequence operation active to serve as a separator for data taken on successive rolls. 1=1A and 1B data taken with internal or external cal lamp powered, or the 1st sample during a S/C roll with the boom sequence operation active
8	parity #1 (parity of science data bytes 7-10)	0=even parity 1=odd parity

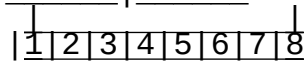


PPR Byte #7

A2.10.5 PPR Science Data 1A &1B. PPR Science Data 1A and 1B (bytes 7-10) contains Rad data, Filter/Retarder positions, calibration lamp status during the data period, boom tag information, 1A &1B parity (as shown in Table A2.10.2) plus 2 (12 bit) scene samples made up of 3 (8 bit) bytes as shown in Table A2.10.3.

Table A2.10.3 Science Data 1A & 1B (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	scene science sample #1A	8 MSBs of a 12 bit word denoting the 1st PP/PH scene science or radiation scene science sample



PPR Byte #8

Table A2.10.3 Science Data 1A & 1B (MSB is bit 1)

Bit(s)	Measurement	Contents
1-4	scene science sample #1A (continued)	4 LSBs of a 12 bit word denoting the 1st PP/PH scene science or radiation scene science sample
5-8	scene science sample #1B	4 MSBs of a 12 bit word denoting the 2nd PP/PH scene science sample of a simultaneously obtained sample pair)or a science temperature sample if 1A is sampling radiation

|1|2|3|4|5|6|7|8| PPR Byte #9

1-8	scene science sample #1B (continued)	8 LSBs of a 12 bit word denoting the 2nd PP/PH scene science sample(of a simultaneously obtained sample pair) or a science temperature sample if 1A is sampling radiation

|1|2|3|4|5|6|7|8| PPR Byte #10

A2.10.6 PPR Science Data 2A & 2B. PPR Science Data 2A and 2B (bytes 11-14) contains data analogous to A2.10.5, Tables A2.10.2 and A2.10.3, denoting the second scene science sample pair of the PPR packet as shown in Figure A2.10.1.

A2.10.7 PPR Science Data 3A & 3B. PPR Science Data 3A and 3B (bytes 15-18) contains data analogous to A2.10.5, Tables A2.10.2 and A2.10.3, denoting the third scene science sample pair of the PPR packet as shown in Figure A2.10.1.

A2.10.8 Telemetry Mode Changes. Upon application of system power, PPR shall configure itself to a normal operating mode. All data shall be valid.

Commanded telemetry mode changes are processed after completion of current mode data acquisition. Mode changes will occur at the start of a MOD 91 count.

A2.11 PLASMA WAVE SUBSYSTEM TELEMETRY

These paragraphs describe the format and content of the PWS output.

PWS data is presented in two forms, the "LPW/LNR Packet" and blocks of "Wide-band Wave-form Receivers" data. The former is a 160-bit (20 byte) parcel described below in A2.11.1; the latter are data blocks of varying sizes that have been fitted to LPW, MPW, MPP, and HPW TDM telemetry formats. Note that the LPW telemetry frame contains sections of both low and high hi-rate PWS data.

A2.11.1 PWS LPW/LNR Packet (Low-rate PWS)

he schematic of a PWS LPW/LNR packet is shown in Figure A2.11.1. One packet is placed in each LPW or LNR frame.

Title	Digital Status	Analog Engineering	Filter Channels	Data Quality	Waveform Survey Data
Data Offset	0	8	16	72	80
Bits/ packet	8	8	56	8	80
Descrip-tion	A2.11.1.2	A2.11.1.3	A2.11.1.4	A2.11.1.5	A2.11.1.6

Figure A2.11.1. PWS LPW/LNR Packet

A2.11.1.1 PWS LPW/LNR Packet Synchronicity. Within the PWS LPW & LNR packets, there will exist two major synchronisms relative to the SCLK. The Digital Status, Analog Engineering, and Spectrum Analyzer Measurement filter channel synchronism relationship to SCLK is shown in Table A2.11.1, while the High Frequency filter channel, and Sweep Frequency Receiver relationship to SCLK is shown in Table A2.11.2.

Table A2.11.1 PWS SI vs. SCLK

SI	RIM (Modulo 4)	MOD 91
0	0	0,4,8,12,16,.....,88
	1	1,5,9,13,17,.....,89
	2	2,6,10,14,18,.....,90
	3	3,7,11,15,19,.....,87
1	0	1,5,9,13,17,.....,89
	1	2,6,10,14,18,.....,90
	2	3,7,11,15,19,.....,87
	3	0,4,8,12,16,.....,88
2	0	2,6,10,14,18,.....,90
	1	3,7,11,15,19,.....,87
	2	0,4,8,12,16,.....,88
	3	1,5,9,13,17,.....,89
3	0	3,7,11,15,19,.....,87
	1	0,4,8,12,16,.....,88
	2	1,5,9,13,17,.....,89
	3	2,6,10,14,18,.....,90

Table A2.11.2 High Frequency filter channel and Sweep Frequency Receiver SI vs. SCLK

SI	RIM (Modulo 4)	MOD 91
0	0	0,28,56,84
	1	21,49,77
	2	14,42,70
	3	7,35,63
1	0	1,29,57,85
	1	22,50,78
	2	15,43,71
	3	8,36,64
2	0	2,30,58,86
	1	23,51,79
	2	16,44,72
	3	9,37,65
3	0	3,31,59,87
	1	24,52,80
	2	17,45,73
	3	10,38,66
4	0	4,32,60,88
	1	25,53,81
	2	18,46,74
	3	11,39,67
5	0	5,33,61,89
	1	26,54,82
	2	19,47,75
	3	12,40,68
6	0	6,34,62,90
	1	27,55,83
	2	20,48,76
	3	13,41,69

SI	RIM (Modulo 4)	MOD 91
7	0	7,35,63
	1	0,28,56,84
	2	21,49,77
	3	14,42,70
8	0	8,36,64
	1	1,29,57,85
	2	22,50,78
	3	15,43,71
9	0	9,37,65
	1	2,30,58,86
	2	23,51,79
	3	16,44,72
10	0	10,38,66
	1	3,31,59,87
	2	24,52,80
	3	17,45,73
11	0	11,39,67
	1	4,32,60,88
	2	25,53,81
	3	18,46,74
12	0	12,40,68
	1	5,33,61,89
	2	26,54,82
	3	19,47,75
13	0	13,41,69
	1	6,34,62,90
	2	27,55,83
	3	20,48,76

Table A2.11.2 High Frequency filter channel and Sweep Frequency Receiver

SI vs. SCLK

SI	RIM (Modulo 4)	MOD 91
14	0	14,42,70
	1	7,35,63
	2	0,28,56,84
	3	21,49,77
15	0	15,43,71
	1	8,36,64
	2	1,29,57,85
	3	22,50,78
16	0	16,44,72
	1	9,37,65
	2	2,30,58,86
	3	23,51,79
17	0	17,45,73
	1	10,38,66
	2	3,31,59,87
	3	24,52,80
18	0	18,46,73
	1	11,39,67
	2	4,32,60,88
	3	25,53,81
19	0	19,47,75
	1	12,40,68
	2	5,33,61,89
	3	26,54,82
20	0	20,48,76
	1	13,41,69
	2	6,34,62,90
	3	27,55,83

SI	RIM (Modulo 4)	MOD 91
21	0	21,49,77
	1	14,42,70
	2	7,35,63
	3	0,28,56,84
22	0	22,50,78
	1	15,43,71
	2	8,36,64
	3	1,29,57,85
23	0	23,51,79
	1	16,44,72
	2	9,37,65
	3	2,30,58,86
24	0	24,52,80
	1	17,45,73
	2	10,38,66
	3	3,31,59,87
25	0	25,53,81
	1	18,46,74
	2	11,39,67
	3	4,32,60,88
26	0	26,54,82
	1	19,47,75
	2	12,40,68
	3	5,33,61,89
27	0	27,55,83
	1	20,48,76
	2	13,41,69
	3	6,34,62,90

A2.11.1.2 Subcommutated Digital Status. The PWS Subcommutated Digital Status section contains one byte (8-bits) of status data. This is shown in Table A2.11.3.

Table A2.11.3 Subcommutated Digital Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1	antenna switch position	0=E 1=B
2-6	filter channel synchronization index	0-27 counter, 28-31=N/A
7	waveform command inhibit/enable	0=enable 1=inhibit
8	spectrum analyzer antenna switch	0=E 1=B

|1|2|3|4|5|6|7|8| SI=0

Bit(s)	Measurement	Contents
1	antenna switch position	0=E 1=B
2-6	filter channel synchronization index	0-27 counter, 28-31=N/A
7	antenna switch inhibit/cycle	0=cycle 1=inhibit
8	calibration enable/inhibit	0=inhibit 1=enable

|1|2|3|4|5|6|7|8| SI=1

Bit(s)	Measurement	Contents
1	antenna switch position	0=E 1=B
2-6	filter channel synchronization index	0-27 counter, 28-31=N/A
7	waveform select switch	0=E 1=B
8	waveform power	0=on 1=off

|1|2|3|4|5|6|7|8| SI=2

Bit(s)	Measurement	Contents
1	antenna switch position	0=E 1=B
2-6	filter channel synchronization index	0-27 counter, 28-31=N/A
7-8	waveform receiver mode	00=waveform survey 01=100.8 kbps 10=806.4 kbps 11=12.6 kbps

|1|2|3|4|5|6|7|8| SI=3

A2.11.1.3 Analog Engineering. The PWS analog engineering section contains one byte (8 bits) of subcommutated data. The contents are shown in Table A2.11.4.

Table A2.11.4 Analog Engineering (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	automatic gain control	0 to 5 volts
1|2|3|4|5|6|7|8 SI=0		
1-8	power supply monitor	0 to 5 volts
1|2|3|4|5|6|7|8 SI=1		
1-8	8 bit analog/digital converter reference 1	0 to 5 volts
1|2|3|4|5|6|7|8 SI=2		
1-8	4 bit analog/digital converter reference 2	0 to 5 volts
1|2|3|4|5|6|7|8 SI=3		

A2.11.1.4 Filter Channels. The Filter Channel section contains 7 bytes of subcommutated data. The contents are shown in Table A2.11.5. 1 byte (byte 4) of this is subcommutated Spectrum Analyzer data. This data is shown in Table A2.11.6. Another 2 bytes (3 and 7) are High Frequency receiver data. It is shown in Table A2.11.7. The other 4 bytes (1,2,5, and 6) are Sweep Frequency Receiver data. They are shown in Table A2.11.8.

Table A2.11.5 Filter Channels (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	sweep frequency receiver subcommutated data	See Table A2.11.8
1|2|3|4|5|6|7|8 Byte 1		
1-8	sweep frequency receiver subcommutated data	See Table A2.11.8
1|2|3|4|5|6|7|8 Byte 2		

Table A2.11.5 Filter Channels (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	high frequency sub-commutated data	See Table A2.11.7

|1|2|3|4|5|6|7|8| Byte 3

Bit(s)	Measurement	Contents
1-8	spectrum analyzer subcommutated data	See Table A2.11.6

|1|2|3|4|5|6|7|8| Byte 4

Bit(s)	Measurement	Contents
1-8	sweep frequency receiver subcommutated data	See Table A2.11.8

|1|2|3|4|5|6|7|8| Byte 5

Bit(s)	Measurement	Contents
1-8	sweep frequency receiver subcommutated data	See Table A2.11.8

|1|2|3|4|5|6|7|8| Byte 6

Bit(s)	Measurement	Contents
1-8	high frequency sub-commutated data	See Table A2.11.7

|1|2|3|4|5|6|7|8| Byte 7

Table A2.11.6 Spectrum Analyzer Data

Spectrum Analyzer SI	Filter Number	Center Frequency (Hz)
0	4	31.1
1	3	17.8
2	2	10.0
3	1	5.62

Table A2.11.7. High Frequency Receiver Data

High Frequency Receiver SI	Receiver Center Frequency (MHz)	
	Byte 3	Byte 7
0	0.1008	0.4032
1	0.1008	0.8060
2	0.2016	1.613
3	0.2016	3.226
4	0.1134	0.4536
5	0.1134	0.9070
6	0.2268	1.814
7	0.2268	3.629
8	0.1260	0.5040
9	0.1260	1.008
10	0.2520	2.016
11	0.2520	4.032
12	0.1386	0.5544
13	0.1386	1.109
14	0.2772	2.218
15	0.2772	4.435
16	0.1512	0.6048
17	0.1512	1.210
18	0.3024	2.419
19	0.3024	4.838
20	0.1638	0.6552
21	0.1638	1.310
22	0.3276	2.621
23	0.3276	5.242
24	0.1764	0.7056
25	0.1764	1.411
26	0.3528	2.822
27	0.3528	5.645

Table A2.11.8 Sweep Frequency Receiver S.I. vs Filter

S.I.	S.F.R.* Byte 6		S.F.R. Byte 5	
	Filt. #	Center Freq. (Hz)	Filt. #	Center Freq. (Hz)
0	1	42.1	29	337
1	2	45.6	30	364
2	3	49.0	31	392
3	4	52.5	32	420
4	5	56.0	33	448
5	6	59.6	34	476
6	7	66.7	35	534
7	8	70.4	36	563
8	9	77.7	37	622
9	10	81.5	38	652
10	11	89.0	39	712
11	12	96.7	40	774
12	13	104.5	41	836
13	14	112.5	42	900
14	15	120.6	43	965
15	16	128.9	44	1031
16	17	137.3	45	1098
17	18	150.2	46	1201
18	19	158.9	47	1272
19	20	172.5	48	1380
20	21	186.4	49	1491
21	22	200.7	50	1606
22	23	215.5	51	1724
23	24	235.9	52	1887
24	25	251.7	53	2013
25	26	268.0	54	2144
26	27	290.6	55	2325
27	28	314.1	56	2513

*Sweep Frequency Receeiver

Table A2.11.8 Sweep Frequency Receiver S.I. vs Filter

S.I.	S.F.R. Byte 2		S.F.R. Byte 1	
	Filt. #	Center Freq. (KHz)	Filt. #	Center Freq. (KHz)
0	57	2.70	85	21.6
1	58	2.91	86	23.3
2	59	3.14	87	25.1
3	60	3.36	88	26.9
4	61	3.58	89	28.7
5	62	3.81	90	30.5
6	63	4.27	91	34.2
7	64	4.50	92	36.0
8	65	4.98	93	39.8
9	66	5.21	94	41.7
10	67	5.70	95	45.6
11	68	6.19	96	49.5
12	69	6.69	97	53.5
13	70	7.20	98	57.6
14	71	7.72	99	61.7
15	72	8.25	100	66.0
16	73	8.78	101	70.3
17	74	9.61	102	76.9
18	75	10.17	103	81.4
19	76	11.04	104	88.3
20	77	11.93	105	95.4
21	78	12.85	106	102.8
22	79	13.79	107	110.3
23	80	15.09	108	120.7
24	81	16.11	109	128.9
25	82	17.15	110	137.2
26	83	18.59	111	148.8
27	84	20.10	112	160.8

A2.11.1.5 Data Quality. This word corresponds to the parity of the Digital Status, the Analog Engineering, and the Filter Channel sections. Each bit represents the parity of one of the 8 preceding words, with the MSB corresponding to the parity of the first word, and so on.

A2.11.1.6 Waveform Survey Data. The Waveform Survey Data section contains 10 bytes of sampled waveform receiver data. If the waveform receiver is in the survey mode (bits 7-8 for SI=2 in Table A2.11.3 equal to 0_{10}), the contents alternate between one sample of data collected at 100.8 Kb/s and one sample of data collected at 12.6 Kb/s, each of which is clocked out over 14 LPW/LNR frames. If bits 2-6 in Table A2.11.3 are 0_{10} to 13_{10} , the data is 12.6 Kb/s data. If bits 2-6 in Table A2.11.3 are 14_{10} to 27_{10} , the data is 100.8 Kb/s data.

If the waveform receiver is in the 12.6 Kb/s mode, the 100.8 Kb/s, or the 806.4 Kb/s mode (bits 7-8 for SI=2 in Table A2.11.3 equal to 3_{10} for 12.6 Kb/s, 1_{10} for 100.8 Kb/s, or 2_{10} for 806.4 Kb/s), the contents of the waveform section are one sample of data collected at the same rate as that of the waveform receiver mode clocked out over 14 LPW frames.

The high-rate PWS data which is sent back in the telemetry frames does not always contain valid and/or complete data. This is due to the varying rates at which the instrument can load and the CDS can pick up high-rate PWS data.

A double buffering method is used to push PWS data through the system. Two buffers are used in the CDS bulk memory, one is referred to as "odd high rate buffer" and the other as "even high rate buffer". They are named after the real-time interrupt counter (RTI) during which data is loaded into them. One RTI is 66-2/3 milliseconds long.

The Phase 2 CDS uses a single unloading scheme. For all telemetry formats, data in the odd buffer is unloaded during even RTIs and the even buffer is unloaded during odd RTIs.

The PWS can load data into the buffers at three different rates depending on the mode of the instrument. In mode 1, data is loaded at 100.8 Kbps, in mode 2 at 806.4 Kbps and in mode 3 at 12.6 Kbps. The CDS picks up the data at different rates depending on the rate of each telemetry format. For Phase 2 there are four possible rates (See Table A2.11.9).

Each buffer is 6720 bits long; however, the CDS does not accept the last 320 bits. The PWS instrument can, and on some occasions does, send 6720 bits to each buffer but CDS only accepts the first 6400 bits.

The buffer address where the data is to be written resets to the beginning of the buffer every RTI. The CDS reads a maximum of 6400 bits at a time, always starting at the beginning of the buffer.

In addition to the above, the spacecraft clock which appears in the header portion of every telemetry frame is ahead by one frame time relative to the observation time for the PWS instrument.

The above condition creates twelve combinations of PWS and CDS rates. Table A2.11.9 summarizes all possible combinations, all lengths are in bits.

Table A2.11.9: PWS Data Formats/Rates

Telemetry Format	Frame Time	PWS in TLM	TLM Frame	PWS Mode	Description
LPW	RTI	1728	5120	1: 6720	1st 1728 picked up next RTI
				2: 53760	1st 1728 picked up next RTI
				3: 840	1st 1728 picked up next RTI, 1st 840 are valid
MPW	RTI	512	1920	1: 6720	1st 512 picked up next RTI
				2: 53760	1st 512 picked up next RTI
				3: 840	1st 512 picked up next RTI
MPP	RTI	1280	1920	1: 6720	1st 1280 picked up next RTI
				2: 53760	1st 1280 picked up next RTI
				3: 840	1st 1280 picked up next RTI, 1st 840 are valid
HPW	RTI	6304	7680	1: 6720	1st 6304 picked up next RTI
				2: 53760	1st 6304 picked up next RTI
				3: 840	1st 6304 picked up next RTI, 1st 840 are valid

Each byte of waveform survey data consists of two 4-bit waveform samples.

A2.11.1A PWS LPW Wideband Packets.

The schematic of a PWS Medium Rate PWS (LPW) packet is shown in Figure A2.11.1A. Four sub-packets are placed in each LPW frame. The four sub-packets are logically concatenated to form a logical LPW PWS data packet of 1728 bits or 432 4-bit data units. (See Table 10A for the data pick-up offsets of the sub-packets within the LPW frame).

Title	Wideband Waveform Receiver Data
Data Offset	0
Bits/packet	432
Description	A2.11.2.2

Figure A2.11.1A. PWS LPW Packet

A2.11.1A.1 PWS LPW Packet Synchronicity. Within the PWS LPW packet, there will exist no synchronism.

A2.11.1A.2 Wideband Waveform Receiver Data. This section contains data from the Wideband Waveform Receiver consisting of 432 words of 4 bits each and is of three possible types. It can be data in the 5 Hz to 1 KHz range (outputting data at 12.6 Kbps), the 50 Hz to 10 KHz range (outputting data at 100.8 Kbps), or the 50 Hz to 80 KHz range (outputting data at 806.4 Kbps). The data contents are determined from the status bits in the LPW packet. These status bits are described in A2.11.1.2. All data is buffered by the CDS, placed into the data stream, with excess bits being discarded.

A2.11.2 PWS MPW Packet

The schematic of a PWS Medium Rate PWS (MPW) packet is shown in Figure A2.11.2. 1 packet is placed in each MPW frame.

Title	Wideband Waveform Receiver Data
Data Offset	0
Bits/packet	512
Description	A2.11.2.2

Figure A2.11.2. PWS MPW Packet

A2.11.2.1 PWS MPW Packet Synchronicity. Within the PWS MPW packet, there will exist no synchronism.

A2.11.2.2 Wideband Waveform Receiver Data. This section contains data from the Wideband Waveform Receiver consisting of 128 words of 4 bits each, and is of three possible types. It can be data in the 5 Hz to 1 KHz range (outputting data at 12.6 kbps), the 50 Hz to 10 KHz range (outputting data at 100.8 kbps), or the 50 Hz to 80 KHz range (outputting data at 806.4 kbps). The data contents are determined from the status bits in the LPW packet, described in A2.11.1.2. All data is buffered by the CDS, placed into the data stream, with excess bits being discarded.

A2.11.3 PWS XPW Packet

DELETED FOR PHASE 2

A2.11.4 PWS HPW Packet

The schematic of a PWS High Rate PWS (HPW) packet is shown in Figure A2.11.4. 1 packet is placed in each HPW frame.

Title	Wideband Waveform Receiver Data
Data Offset	0
Bits/ packet	6304
Description	A2.11.4.2

Figure A2.11.4. PWS HPW Packet

A2.11.4.1 PWS HPW Packet Synchronicity. Within the PWS HPW packet, there will exist no synchronism.

A2.11.4.2 Wideband Waveform Receiver Data. This section contains data from the Wideband Waveform Receiver consisting of 1576 words of 4 bits each, and is of two possible types. It can be data in the 50 Hz to 10 KHz range (outputting data at 100.8 kbps), or the 50 Hz to 80 KHz range (outputting data at 806.4 kbps). The data contents are determined from the status bits in the LPW packet, described in A2.11.1.2. All data is buffered by the CDS, placed into the data stream, with excess bits being discarded.

A2.11.5 PWS PW4 Packet

DELETED FOR PHASE 2

A2.11.6 PWS PW8 Packet

DELETED FOR PHASE 2

A2.11.7 PWS MPP Packet

The schematic of a PWS Medium rate PWS (MPP) packet is shown in Figure A2.11.7. A single packet is placed in each MPP frame.

Title	Wideband Waveform Receiver Data
Data Offset	0
Bits/ packet	1280
Description	A2.11.7.2

Figure A2.11.7. PWS MPP Packet

A2.11.7.1 PWS MPP Packet Synchronicity. Within the PWS/MPP packet, there will exist no synchronism.

A2.11.7.2 Wideband Waveform Receiver Data. This section contains data from the Wideband Waveform Receiver consisting of 320 words of 4 bits each, and is of three possible types. It can be data in the 5 Hz to 1 KHz range (outputting data at 100.8 Kbps). The data contents are determined from the status bits in the LPW packet, described in A2.11.1.2. All data is buffered by the CDS, placed into the data stream, with excess bits being discharged.

A2.11.8 PWS HCJ Packet

DELETED FOR PHASE 2

A2.11.9 PWS HPJ Packet

DELETED FOR PHASE 2

A2.12 SOLID STATE IMAGING SUBSYSTEM TELEMETRY

This paragraph describes the format and content of the SSI output, both to the LPW/LNR data stream via the Data System Bus and to the DBUM via the high rate interface.

A2.12.1 SSI LPW/LNR Packet. The schematic of this packet is shown in Figure A2.12.1. Three identical SSI LPW/LNR packets are placed in each frame, 96 bits per frame.

Title	Standard Housekeeping Data	2 1/3 Second Imaging Housekeeping Data
Data Offset	0	16
Bits/packet	16	16
Description	A2.12.1.2	A2.12.1.3

Figure A2.12.1 SSI LPW/LNR Packet

A2.12.1.1 Instrument Synchronicity. Within the SSI LPW/LNR packet, there will exist two major synchronisms relative to the SCLK. The relationship of the Synchronization Index's to MOD 91 count is shown in Table A2.12.1.

Table A2.12.1 Relationship of SI's to MOD 91

Standard Imaging SI	MOD 91
0	0, 13, 26, 39, 52, 65, 78
1	1, 14, 27, 40, 53, 66, 79
2	2, 15, 28, 41, 54, 67, 80
3	3, 16, 29, 42, 55, 68, 81
4	4, 17, 30, 43, 56, 69, 82
5	5, 18, 31, 44, 57, 70, 83
6	6, 19, 32, 45, 58, 71, 84
7	7, 20, 33, 46, 59, 72, 85
8	8, 21, 34, 47, 60, 73, 86
9	9, 22, 35, 48, 61, 74, 87
10	10, 23, 36, 49, 62, 75, 88
11	11, 24, 37, 50, 63, 76, 89
12	12, 25, 38, 51, 64, 77, 90

Table A2.12.1 Relationship of SI's to MOD 91

2 1/3 Second Imaging SI	MOD 91
0	0, 7, 14, 21, 28, 35, 42, 49, 56, 63, 70, 77, 84
1	1, 8, 15, 22, 29, 36, 43, 50, 57, 64, 71, 78, 85
2	2, 9, 16, 23, 30, 37, 44, 51, 58, 65, 72, 79, 86
3	3, 10, 17, 24, 31, 38, 45, 52, 59, 66, 73, 80, 87
4	4, 11, 18, 25, 32, 39, 46, 53, 60, 67, 74, 81, 88
5	5, 12, 19, 26, 33, 40, 47, 54, 61, 68, 75, 82, 89
6	6, 13, 20, 27, 34, 41, 48, 55, 62, 69, 76, 83, 90

A2.12.1.2 SSI Standard Housekeeping Data. The SSI Standard Housekeeping Data section contains 26 data words which are commutated into the first two (of four) data bytes in each LPW/LNR Frame, as shown in Table A2.12.2. The contents of the SSI Housekeeping Data words are shown in Table A2.12.3. The subcommutated housekeeping data is shown in Table A2.12.4.

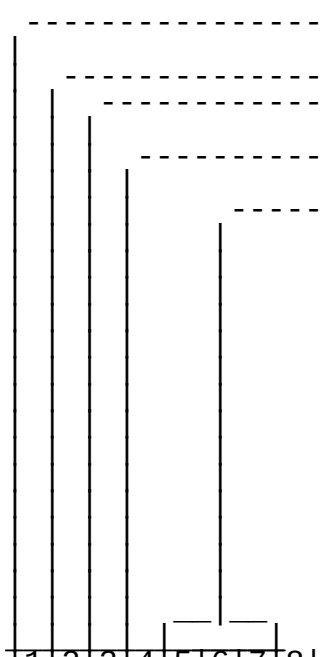
Table A2.12.2 SSI Standard Housekeeping vs. SI(MSB is bit 1)

Standard Imaging SI	Byte 1	Byte 2
0	Data Word 1	Data Word 2
1	Data Word 3	Data Word 4
2	Data Word 5	Data Word 6
3	Data Word 7	Data Word 8
4	Data Word 9	Data Word 10
5	Data Word 11	Data Word 12
6	Data Word 13	Data Word 14
7	Data Word 15	Data Word 16
8	Data Word 17	Data Word 18
9	Data Word 19	Data Word 20
10	Data Word 21	Data Word 22
11	Data Word 23	Data Word 24
12	Data Word 25	Data Word 26

Table A2.12.3 SSI Housekeeping Data (MSB is bit 1)

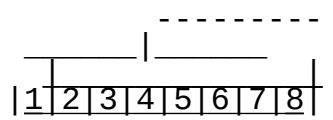
	Bit(s)	Measurement	Contents
1 2 3 4 5 6 7 8	1-8	subcommutated data	
SSI Housekeeping Data Word 1			
1 2 3 4 5 6 7 8	1-8	programmed memory word readout	DN of word addressed by readout
SSI Housekeeping Data Word 2			

Table A2.12.3 SSI Housekeeping Data (MSB is bit 1)



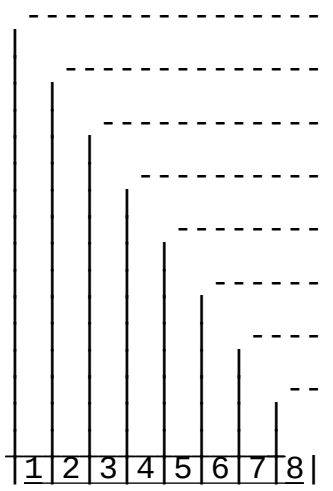
Bit(s)	Measurement	Contents
1	engineering sample mode	0=normal 1=programmed
2	spare	
3	light flood internal disable	0=enabled 1=disabled
4	light flood status	0=off 1=on
5-8	programmed engrng channel: if engrng sample mode is programmed, data in words 6 through 21 are replaced with 16 samples of the indicated measurement	0000=word 6 0001=word 7 0010=word 8 0011=word 9 0100=word 10 0101=word 11 0110=word 12 0111=word 13 1000=word 14 1001=word 15 1010=word 16 1011=word 17 1100=word 18 1101=word 19 1110=word 20 1111=word 21

SSI Housekeeping Data Word 3



1-8	engineering start time	0-129 RTI

SSI Housekeeping Data Word 4



1	bus parity error detected	0=no error detected 1=error detected
2	state vector control program links	0=ROM links 1=scratchpad links
3	state vector control program memory status	0=ROM 1=RAM
4	state vector control scratchpad status	0=scratchpad 1 1=scratchpad 2
5	timing sync error	0=no error detected 1=error detected
6	unrecognized cmd detected	0=no error detected 1=error detected
7	secondary scratchpad error	0=no error detected 1=error detected
8	primary scratchpad error (SP1)	0=no error detected 1=error detected

SSI Housekeeping Data Word 5

Table A2.12.3 SSI Housekeeping Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	input current	0 to 512 ma rms

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 6

Bit(s)	Measurement	Contents
1-8	+50 Vdc	0 to 61 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 7

Bit(s)	Measurement	Contents
1-8	+15 Vdc	0 to 22 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 8

Bit(s)	Measurement	Contents
1-8	-15 Vdc	0 to -22 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 9

Bit(s)	Measurement	Contents
1-8	+10 Vdc	0 to 16 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 10

Bit(s)	Measurement	Contents
1-8	+5 Vdc	0 to 10 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 11

Bit(s)	Measurement	Contents
1-8	-5 Vdc	0 to -10 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 12

Bit(s)	Measurement	Contents
1-8	CCD heater voltage	0 to 14 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 13

Bit(s)	Measurement	Contents
1-8	CCD temperature, fine	-97.2 to -122.8 deg. C

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 14

Bit(s)	Measurement	Contents
1-8	baseline correction volts	-7.5 to +7.5 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 15

Table A2.12.3 SSI Housekeeping Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	ADC reference volts	0 to -15.3 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 16

Bit(s)	Measurement	Contents
1-8	VDD	0 to 42.6 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 17

Bit(s)	Measurement	Contents
1-8	VREF	0 to 42.6 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 18

Bit(s)	Measurement	Contents
1-8	CCD temp, coarse	+55 to -150 degrees C

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 19

Bit(s)	Measurement	Contents
1-8	positive clock volts	0 to +15.2 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 20

Bit(s)	Measurement	Contents
1-8	negative clock volts	0 to -32.0 Vdc

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 21

Bit(s)	Measurement	Contents
1-8	picture count	increments every non-zero exposure and dark current calibration

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 22

Bit(s)	Measurement	Contents
1-8	image parameters 1	cmd echo of image param.

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 23

Bit(s)	Measurement	Contents
1-8	image parameters 2	cmd echo of image param.

1	2	3	4	5	6	7	8

SSI Housekeeping Data Word 24

Table A2.12.3 SSI Housekeeping Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-3	imaging mode	000=60-2/3 s 010=8-2/3 s 100=30-1/3 s 101=15-1/6 s 110=2-1/3 s
4	long exposure cycle	0=cycle 1 1=cycle 2
5	compression mode	0=rate controlled 1=information preserving
6	image compressor	0=compressor out 1=compressor in
7-8	gain	00=gain 1 01=gain 2 10=gain 3 11=gain 4

|1|2|3|4|5|6|7|8| SSI Housekeeping Data Word 25

1	memory write protect	0=write protect off 1=write protect on
2	parallel clock state	0=normal 1=inverted
3	watchdog timer	0=not tripped 1=tripped
4	blemish protection	0=off 1=on
5-7	actual filter position	position 0 through 7
8	filter pstn parity	odd parity

|1|2|3|4|5|6|7|8| SSI Housekeeping Data Word 26

Table A2.12.4 SSI Subcommutated Housekeeping Data (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	MS byte programmed memory word address	

|1|2|3|4|5|6|7|8| MOD91=0 Subcommutated SSI Housekeeping Data Word 1

Bit(s)	Measurement	Contents
1-8	LS byte programmed memory word address	

|1|2|3|4|5|6|7|8| MOD91=13 Subcommutated SSI Housekeeping Data Word 1

Table A2.12.4 SSI Subcommutated Housekeeping Data (MSB is bit 1)

	Bit(s)	Measurement	Contents
1|2|3|4|5|6|7|8 MOD91=26 Subcommutated SSI Housekeeping Data Word 1	1-4	parity error count	count of parity errors
	5-8	unrecognized cmd count	count of unrecognized commands
1|2|3|4|5|6|7|8 MOD91=39 Subcommutated SSI Housekeeping Data Word 1	1-8	MS byte SSI transfer count	MS byte, number of bytes received from CDS
1|2|3|4|5|6|7|8 MOD91=52 Subcommutated SSI Housekeeping Data Word 1	1-8	LS byte SSI transfer count	LS byte, number of bytes received from CDS
1|2|3|4|5|6|7|8 MOD91=65 Subcommutated SSI Housekeeping Data Word 1	1-8	primary program memory checksum (ROM)	result of ROM checksum
1|2|3|4|5|6|7|8 MOD91=78 Subcommutated SSI Housekeeping Data Word 1	1-8	secondary program memory checksum (RAM)	result of RAM checksum

A2.12.1.3 SSI 2 1/3 Second Imaging Housekeeping Data. When the SSI is in the 2 1/3 Second Imaging mode (word 25, bits 1-2=11), the SSI 2 1/3 Second Imaging Housekeeping Data section contains 5 data words (from Table A2.12.3) which are commutated into the second two (of four) data bytes in each LRS Frame, as shown in Table A2.12.5. When the SSI is not in the 2 1/3 Second Imaging mode, the SSI 2 1/3 Second Imaging Housekeeping Data section contents are invalid.

Table A2.12.5 SSI 2 1/3 Second Imaging Housekeeping vs. SI(MSB is bit 1)

2 1/3 Second Imaging SI	Byte 3	Byte 4
0	Data Word 22	Data Word 23
1	Data Word 24	Data Word 25
2	Data Word 26	spare
3	spare	spare
4	Data Word 22	Data Word 23
5	Data Word 24	Data Word 25
6	Data Word 26	spare

A2.12.1.4 Telemetry Mode Changes. Upon the application of system power, SSI shall assume a valid imaging mode, with the microprocessor configured to ROM program and scratchpad memory one. The SSI shall inhibit shuttering, filter wheel stepping, and insure that the shutter is closed until valid commanding takes place. Upon the removal of system power, the SSI shall prevent shuttering, filter wheel stepping, and insure that the shutter is closed. Commanded telemetry mode changes shall be processed every RTI. Telemetry imaging mode changes shall occur at the beginning of a RIM.

A2.12.2 SSI 67.2 Kbps XCM Packet.

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A2.12.2A SSI 67.2 Kbps XED Packet.

DELETED FOR PHASE 2

A2.12.3 SSI 115.2 Kbps Standard Imaging Packet. The schematic of this packet is shown in Figure A2.12.4. One SSI 115.2 kbps standard imaging packet is divided among 910 115.2 kbps frames (one image line per frame).

Title	Fill Data	Image Data Section
Data Offset	0	693440
Bits/packet	693440 (lines 0-109)	5043200 (lines 110-909)
Description	A2.12.3.2	A2.12.3.4

Figure A2.12.4 SSI 115.2 Kbps Packet

A2.12.3.1 Instrument Synchronicity. Within the SSI 115.2 kbps standard imaging packet, there will exist no major synchronism relative to the SCLK.

A2.12.3.2 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.3.3 Deleted

A2.12.3.4 Image Data Section. This section contains standard imaging. Each 6304 bits of data makes up one line of an image. Each 8 bits of data corresponds to one pixel of the image.

A2.12.3.5 Extended Exposure Mode. In the Extended Exposure Mode, two packets of image data are required for each image. The first packet will contain data as specified before, but the first packet's image data will not be valid (i.e. it will contain fill data), and the image data will all be present in the second packet's image data area.

A2.12.4 SSI 115.2 Kbps Compressed Imaging Packet. The schematic of this packet is shown in Figure A2.12.6. One SSI 115.2 kbps compressed imaging packet is divided among 910 115.2 kbps frames (two image lines per frame).

Title	Last line of previous image 2	Fill Data	First line of image 1	Fill Data	Subsequent Image Lines Section 1	Last line of Image 1	Fill Data	First line of Image 2	Fill Data	Subsequent Image Lines Section 2
Data Offset	0	3104	346720	349824	353024	2871424	2871424	3215040	3218144	3221344
Bits/ Packet	3104 (line 0)	343616 (last half of line 0-54)	3104 (55)	3200 (last half of line 55)	2515296 (56-454)	3104 (455)	343616 (last half of line 455-509)	3104 (510)	3200 (last half of line 510)	2515296 (511-909)
Description	A2.12.4.4	A2.12.4.2	A2.12.4.4	A2.12.4.2	A2.12.4.4	A2.12.4.4	A2.12.4.5	A2.12.4.7	A2.12.4.5	A2.12.4.7

Figure A2.12.6 SSI 115.2 kbps Compressed Imaging Packet

A2.12.4.1 Instrument Synchronicity. Within the SSI 115.2 kbps compressed imaging packet, there will exist no major synchronism relative to the SCLK.

A2.12.4.2 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.4.3 Deleted

A2.12.4.4 Image Data Section #1. This section contains compressed imaging. Each 115.2 kbps frame of imaging data contains 2 sets of compressed image data (2592 bits) and Reed-Solomon parity symbols (512 bits), and filler data (96 bits). Each of the sets of compressed image data and Reed-Solomon parity symbols is as described in paragraph A2.12.2.5 and A2.12.2.6. Because of compressed line timing delays, each line of each image is delayed one line time.

A2.12.4.5 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.4.6 Deleted

A2.12.4.7 Image Data Section #2. This section contains compressed imaging. Each 115.2 kbps frame of imaging data contains 2 sets of compressed image data (2592 bits) and Reed-Solomon parity symbols (512 bits), and filler data (96 bits). Each of the sets of compressed image data and Reed-Solomon parity symbols is as described in paragraph A2.12.2.5 and A2.12.2.6. Because of compressed line timing delays, each line of each image is delayed one line time, and the last line of each packet is delayed until the start of the following packet.

A2.12.4.8 Extended Exposure Mode. In the Extended Exposure Mode, two groups of image data are required for each image. The first group will contain data as specified before, but the first group's image data will not be valid (i.e. it will contain fill data), and the image data will all be present in the second group's image data area.

A2.12.5 SSI 403.2 Kbps Compressed Imaging Packet. The schematic of this packet is shown in Figure A2.12.8. One SSI 403.2 kbps compressed imaging packet is divided among 7280 403.2 kbps frames.

Title	Image #1	Image #2	Image #3	Image #4	Image #5	Image #6	Image #7
Start Bit	1	3228161	6456321	9684481	12912641	16140801	19368961
Stop Bit	3228160	6456320	9684480	12912640	16140800	19368960	22597120

Figure A2.12.8 SSI 403.2 kbps Compressed Imaging Packet

Seven images are in each packet. The relationship between the start of each image, and the SCLK is shown in Table A2.12.4.

Table A2.12.6 Relationship of MOD 91 to start of Image

Image Start	MOD 91
Image #1	0
Image #2	13
Image #3	26
Image #4	39
Image #5	52
Image #6	65
Image #7	78

The format of each image is shown in Figure A2.12.9.

Title	Last line of previous Image	Fill Data	Image Data Section
Bits/image	3104 (line 0)	744960 (lines 1-240)	2480096 (lines 241-1039)
Description	A2.12.5.4	A2.12.5.2	A2.12.5.4

Figure A2.12.9 SSI 403.2 kbps Image Area

A2.12.5.1 Instrument Synchronicity. Within the SSI 403.2 kbps standard imaging packet, there will exist no major synchronism relative to the SCLK.

A2.12.5.2 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.5.3 Deleted

A2.12.5.4 Image Data Section. This section contains compressed imaging. Each 3104 bits of data contains 2592 bits of compressed image data and 512 bits of Reed-Solomon parity symbols. Each of the sets of compressed image data and Reed-Solomon parity symbols is as described in paragraph A2.12.2.5 and A2.12.2.6. Because of delays in compressed line timing, the last line of each image is delayed until the start of the following Image Area.

A2.12.5.5 Extended Exposure Mode. In the Extended Exposure Mode, two groups of image data are required for each image. The first group will contain data as specified before, but the first group's image data will not be valid (i.e. it will contain fill data), and the image data will all be present in the second group's image data area.

A2.12.6 SSI 806.4 Kbps Standard Imaging Packet. The schematic of this packet is shown in Figure A2.12.11. One SSI 806.4 kbps standard imaging packet is divided among 7280 806.4 kbps frames.

Title	Image #1	Image #2	Image #3	Image #4	Image #5	Image #6	Image #7
Start Bit	1	6656001	13312001	19968001	26624001	33280001	39936001
Stop Bit	6656000	13312000	19968000	26624000	33280000	39936000	46592000

Figure A2.12.11 SSI 806.4 kbps Standard Imaging Packet

Seven images are in each packet. The relationship between the start of each image, and the SCLK is shown in Table A2.12.4.

The format of each image is shown in Figure A2.12.12.

Title	Fill Data	Image Data Section
Bits/image	1536000 (lines 0-239)	5120000 (lines 240-1039)
Description	A2.12.6.2	A2.12.6.4

Figure A2.12.12 SSI 806.4 kbps Image Area

A2.12.6.1 Instrument Synchronicity. Within the SSI 806.4 kbps standard imaging packet, there will exist no major synchronism relative to the SCLK.

A2.12.6.2 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.6.3 Deleted

A2.12.6.4 Image Data Section. This section contains standard imaging. Each 6400 bits of data makes up one line of an image. Each 8 bits of image data makes up one pixel of image data.

A2.12.6.5 Extended Exposure Mode. In the Extended Exposure Mode, two groups of image data are required for each image. The first group will contain data as specified before, but the first groups image data will not be valid (i.e. it will contain fill data), and the image data will all be present in the second groups image data area.

A2.12.7 SSI 806.4 Kbps Averaged Imaging Packet. The schematic of this packet is shown in Figure A2.12.14. One SSI 806.4 kbps averaged imaging packet is divided among 7280 806.4 kbps frames.

Title	26 Averaged Images
Data Offset	0
Bits/packet	46592000

Figure A2.12.14 SSI 806.4 kbps Averaged Imaging Packet

Twenty six images are in each packet. The relationship between the start of each image, and the SCLK is shown in Table A2.12.6.

Table A2.12.7. SCLK vs. Image Start

Image Start	MOD91
1	0
2	4
3	7
4	11
5	14
6	18
7	21
8	25
9	28
10	32
11	35
12	39
13	42
14	46
15	49
16	53
17	56
18	60
19	63
20	67
21	70
22	74
23	77
24	81
25	84
26	88

The format of each odd image is shown in Figure A2.12.15, and the format of each even image is shown in Figure A2.12.16.

Title	Fill Data	Image Data Section	Fill Data
Bits/image	512000 (lines 0-159)	1280000 (lines 160-559)	256000 (lines 560-639)
Description	A2.12.7.2	A2.12.7.4	A2.12.7.2

Figure A2.12.15 SSI 806.4 kbps Averaged Image Area (odd image)

Title	Fill Data	Image Data Section
Bits/image	256000 (lines 0-79)	1280000 (lines 80-479)
Description	A2.12.7.2	A2.12.7.4

Figure A2.12.16 SSI 806.4 kbps Averaged Image Area (even image)

A2.12.7.1 Instrument Synchronicity. Within the SSI 806.4 kbps averaged imaging packet, there will exist no major synchronism relative to the SCLK.

A2.12.7.2 Fill Data. This section contains fill data composed of data already present in the data buffers.

A2.12.7.3 Deleted

A2.12.7.4 Image Data Section. This section contains standard imaging. Each 3200 bits of data makes up one line of an image. Each 8 bits of image data makes up one pixel of image data.

A2.12.7.5 Extended Exposure Mode. In the Extended Exposure Mode, two groups of image data are required for each image. The first group will contain data as specified before, but the first groups image data will not be valid (i.e. it will contain fill data), and the image data will all be present in the second groups image data area.

A2.13 ULTRAVIOLET SPECTROMETER SUBSYSTEM TELEMETRY

These paragraphs describe the format and content of the UVS output.

A2.13.1 UVS Packet. The schematic of the UVS packet is shown in Figure A2.13.1. 6.5 LPW/LNR/LPU frames are required to transport 1 UVS packet (scan).

	4368 Bits (546 Bytes)			
Title	Sync Code	Digital Status	Analog Eng.	UVS Sci. Data
Data offset	0	56	80	144
Bits/packet	56	24	64	4224
Description	A2.13.3	A2.13.4	A2.13.5	A2.13.6

Figure A2.13.1. UVS Packet (scan)

A2.13.2 Instrument Synchronicity. There are 14 UVS packets (scans) per RIM. The first LPW/LNR/LPU frame of each RIM is all zero's. The first UVS data scan then starts in the second frame, and the 14th UVS data scan is truncated by one LPW/LNR/LPU frame. The relationship between the start of the UVS packet and the Synchronization Index and SCLK is shown in Table A2.13.1. The length of the scan (4-1/3 sec) is chosen to coincide with the NIMS scan.

Table A2.13.1 UVS packet start vs. SCLK

Bit 1 of UVS packet within packet position in LPW/LNR/LPU frames

SI	MOD 91	Byte
1	1	1
2	7	43
3	14	1
4	20	43
5	27	1
6	33	43
7	40	1
8	46	43
9	53	1
10	59	43
11	66	1
12	72	43
13	79	1
14	85	43

A2.13.3 Sync Code. The contents of the sync code section are 7 bytes of sync words. Each byte is a 1111 1111.

A2.13.4 Digital Status. The contents of the digital status section are shown in Table A2.13.2.

Table A2.13.2 UVS Digital Status (MSB is bit 1)

Bit(s)	Measurement	Contents
1-8	Starting wavelength	wavelength 0-255

|1|2|3|4|5|6|7|8| UVS Byte #8

Bit(s)	Measurement	Contents
1	F-detector status	0 = off 1 = on
2	N-detector status	0 = off 1 = on
3	G-detector status	0 = off 1 = on
4	F-detector high voltage status	0 = on 1 = off
5	N-detector high voltage status	0 = on 1 = off
6	G-detector high voltage status	0 = on 1 = off
7-8	Integration time	00= short (approx. 2 ms) 01= long (approx. 6 ms) 10= short (approx. 1 ms) 11= long (approx. 4 ms)

|1|2|3|4|5|6|7|8| UVS Byte #9

Bit(s)	Measurement	Contents
1	Wavelength scan	0 = scan grating 1 = fix grating
2-3	Wavelength monitored	00= first position monitored (or scanning if mode=0) 01= second position monitored 10= third position monitored 11= fourth position monitored
4	Grating	0 = motor control grating #1 1 = motor control grating #2
5	Micro-P control	0 = (cold start) UVS not under microprocessor control 1 = UVS under micro-processor control
6	Detectors high voltage state	0 = HV on for selected channel 1 = HV off for all channels
7	stim lamp status	0 = off 1 = on
8	limb override/ sensor status	0 = override off 1 = override on

|1|2|3|4|5|6|7|8| UVS Byte #10

A2.13.5 Analog Engineering Status. The contents of the analog engineering status section are shown in Table A2.13.3

Table A2.13.3 UVS Analog Engineering Status

Byte	Measurement
11	low voltage +10 v.
12	low voltage +5 v.
13	high voltage F
14	high voltage N
15	high voltage G
16	logic temperature
17	detector temperature
18	limb sensor

A2.13.6 UVS Science Data. The N and G channels consist of 8 bit linear count data. The F channel is a 15 bit data word log compressed to 8 bit count data. The algorithms for the data compression and reconstruction are show in Figure A2.13.2. The science data for one UVS packet (scan) consists of 528 (8 bit) bytes read consecutively, beginning with byte 19 bit 1 of the packet (scan). Each 4-1/3 sec. packet (scan) contains data from one sensor only (N, G, or F). The engineering parameter, Table A2.13.2 byte 9, bits 1-3, at the beginning of each packet (scan) tells which sensor is active during that scan.

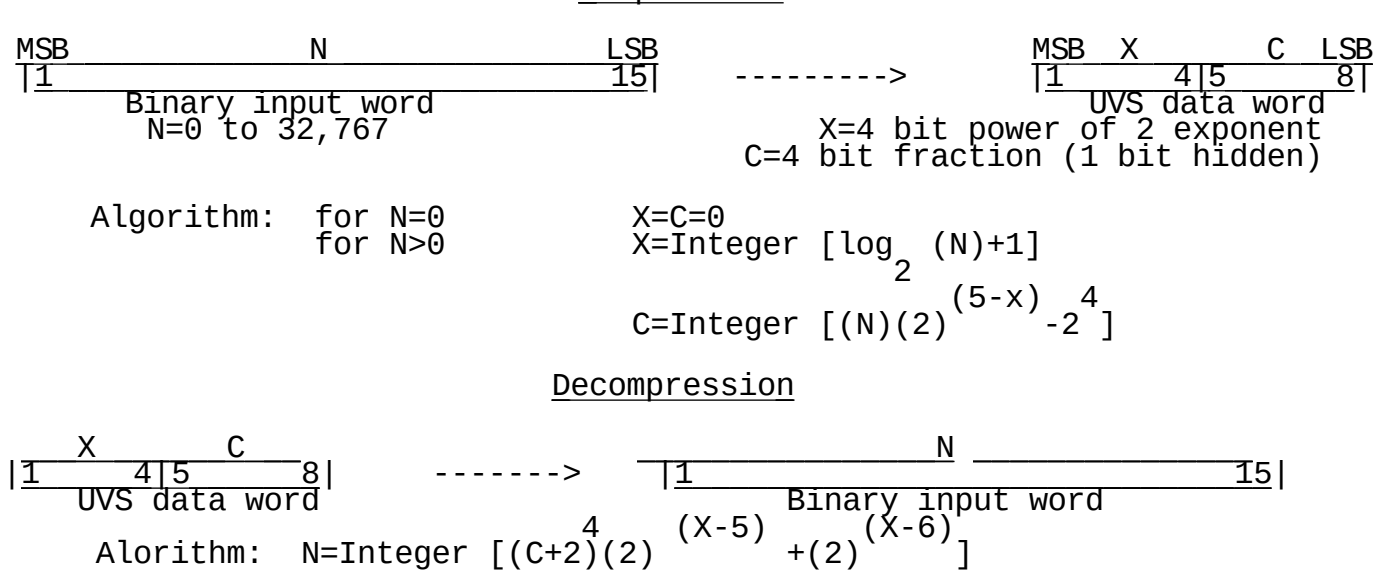

Figure A2.13.2
UVS compression/decompression Process

A2.13.7 Telemetry Mode Changes. Upon application of system power, UVS shall automatically configure itself to an operational mode identical to paragraph A2.13.1. All data shall be valid, but not sychronized to RTI or RIM. The 4-1/3 sec. packet (scan) can start at any byte boundary within any MOD 91 count, therefore table A2.13.1 does not apply during POR (power on reset).

Commanded telemetry mode changes are processed every RIM. Mode changes data update shall occur one LPW/LNR/LPU frame after the start of a RIM.

A2.14 RELAY RADIO HARDWARE

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A2.15 OPEN ITEMS AND TBD'S.

All TBD items in this document are listed in Table A2.15.1. All known open items are listed in Table A2.15.2.

Table A2.15.1. GLL-3-280 TBD Items

PAGE	IDENTIFICATION	ITEM	RESPONSIBLE ENGINEER	REQUIRED CLOSURE DATE
	A2.2.14.2.2	Phase 2 Variable Packet Definitions	Unassigned	
		SSI Packet Formats for HMA, HCA, HIS TDM TLM	Unassigned	
		NIMS Packet Formats for LNR & LPU TDM TLM	Unassigned	

Table A2.15.2. GLL-3-280 Open Items

PAGE	IDENTIFICATION	ITEM	RESPONSIBLE ENGINEER	REQUIRED CLOSURE DATE
		NONE		

PHASE 2 REVISION PAGE

Revision	Date	ECRs Incorporated	Comments
Change 1 (was Chg 3)	8 March 1994	35557	PHASE 2 - Rev. A of Appendix C
Change 2 (was Chg 4)	21 December 94	35557, 35565, 35566, 35567, 35581, 35582, 35587, 35593	PHASE 2 Update Specifications - Appendix D
Revision D	15 Aug 1995	35607, 35611, 35614, 35615, 35624	PHASE 2 - New Appendix D